NEW ASYMMETRICAL MULTILEVEL INVERTER BASED DYNAMIC VOLTAGE RESTORER

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Abstract: *In this paper, a new topology for multilevel converter based on sub-multilevel converter units and full-bridge converters is proposed. The proposed topology significantly reduces the number of dc voltage sources and switches as the number of output voltage levels increases. To synthesize maximum levels at the output voltage and to reduce the total harmonic distortion (THD), three different control strategies are proposed. The operation and performance of the proposed multilevel converter have been analysed and simulated in the MATLAB software and the results are presented for single-phase 25-level converter. Dynamic Voltage Restorer is a power electronic device that is used to inject 3-phase voltage in series and in synchronism with the distribution feeder voltages in order to compensate voltage sag. The principle component of the DVR is a voltage source inverter that generates three phase voltage and provides the voltage support to a sensitive load during voltage sags. The improved version of proposed multilevel inverter with reduced THD is used in DVR to compensate the voltage sag in power system and if any fault occurs in power system thereby reduce the voltage variation in distribution side. Simulation of DVR has been developed by using Matlab/Simulink.*

Key words: *Asymmetric Multilevel Inverter, DVR, ISPWM, MSPWM, SHPWM, THD.*

1. Introduction

The basic concept of a multilevel converter is to use a series of power semiconductor switches that properly connected to several lower dc voltage sources to synthesize a near sinusoidal staircase voltage waveform. The small output voltage step results in high quality output voltage, reduction of voltage stresses on power switching devices, lower switching losses and higher efficiency. Numerous multilevel converter topologies and wide variety of control methods have been developed in [1]-[4]. Three different basic multilevel converter topologies are the neutral point clamped (NPC) or diode clamped [5-6], the flying capacitor (FC) or capacitor clamped and the cascaded H-bridge (CHB). The main drawbacks of NPC topology are their unequal voltage sharing among series connected capacitors that result in dc-link capacitor unbalancing and requiring a great number of clamping diodes for higher level. The FC multilevel converter uses flying capacitor as clamping devices. These topologies have several attractive properties in comparison with the NPC converter, including the advantage of the transformerless operation and redundant phase leg states that allow the switching stresses to be equally distributed between semiconductor switches. But, these converters require an excessive number of storage capacitors for higher voltage steps. The CHB topologies are proper option for high level applications from point of view of modularity and simplicity of control. But, in this topology, a large number of isolated dc voltage sources are required to supply each conversion cell. It increases the converter cost and complexity.

In multilevel converter, the power quality is improved as the number of levels increases at the output voltage. However, it causes to the increasing number of switching devices and other components, and increases the cost and control complexity and tends to reduce the overall reliability and efficiency of the converter. It is noticeable that multilevel converters can sustain the operation in case of internal fault. In the case of internal fault of one cell of FC converter, the maximum output voltage remains constant, but the number of levels decreases. On the other hand, when an internal fault is detected in the CHB converter, and the faulty cell is identified, it can be easily isolated through an external switch and replaced by a new operative cell [7].

Asymmetric and/or hybrid multilevel converters have been presented in [8]. In the asymmetric topologies, the values of dc voltage sources magnitudes are unequal or changed dynamically [9]. These converters reduce the

size and cost of the converter and improve the reliability since fewer semiconductors and capacitors are employed [10]. The hybrid multilevel converters are composed of different multilevel topologies with unequal values of dc voltage sources and different modulation techniques and/or semiconductor technologies [8]. With appropriate selection of switching devices, the converter cost is significantly reduced. But, the application of different multilevel topologies result in loss of modularity and produces problems with switching frequency and restrictions on the modulation and control method [11].

The researchers are strived in [12] to introduce a new topology for multilevel converters with a reduced number of components compared to conventional multilevel converters. This topology is composed of modular sub multilevel converters that makes it easily extensible to higher number of output voltage levels without undue increase in the power circuit complexity and reduces controller design cost. By the presented algorithm in [12], it is not possible to create all levels (odd and even) at the output voltage, and it reduces the flexibility of the converter. Also, to create the output voltage with a constant number of levels, the converter needs many large numbers of bidirectional switches. To overcome these disadvantages, [13] has presented a new topology, which has decreased the number of bidirectional switches and dc voltage source compared to [12] and with the ability of the production of all levels at the output voltage. The main drawback of this topology is the utilization of unidirectional switches that operate in the high output voltage.

The structures, based on similar concepts, have been presented in [14-15]. In these topologies, the dc source is formed by connecting a number of half-bridge cells, diode-clamped phase leg or capacitor-clamped phase leg. Also, in [16-18], the topology has been obtained from the mixture of the FC and CHB inverter. These structures provide a high number of output levels using low number of components. But, the main drawback of these topologies is the utilization a full-bridge converter, which operates in the high output voltage. Also, these designs are not flexible.

This paper proposes a new modular and simple topology for cascaded multilevel converter that produces a high number of levels with the application of a low number of power electronic components. Then, a procedure for calculating the values of required dc voltage sources is also proposed. In addition, the structure of the proposed topology is optimized for various aims. Finally, a design example of the proposed multilevel converter is included.

2. Proposed Multilevel Converter

The basic unit of the sub multilevel converter, is presented in [19-20], is illustrated in Fig. 1(a). It consists of several dc voltages and bidirectional switches. If n voltage sources are used, n+ 1 different value can be obtained for v_o, by n + 1 bidirectional switches. The output voltage of this sub multilevel converter has zero or positive values. The presented unit requires bidirectional switches with the capability of blocking voltage and conducting current in both directions. Several arrangements can be used to create bidirectional switches.

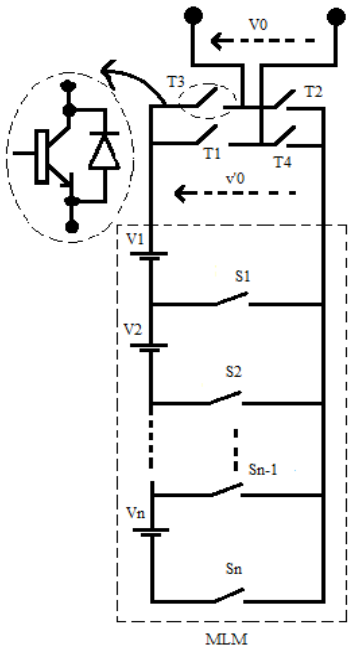

Fig. 1(a): Proposed Multilevel Inverter

The proper configuration of bidirectional switches is arranged by a common emitter connection of two IGBTs, with each one of IGBTs has an anti parallel diode. Because the emitters of two IGBTs are common, the base voltage of each IGBT can be measured versus its common emitter. Therefore, a bidirectional switch requires a gate driver circuit in this configuration. This configuration of bidirectional switch is used in this paper, to make it comparable with one presented in [19-20]. The typical output waveform is shown in “Fig. 1 (b)”.

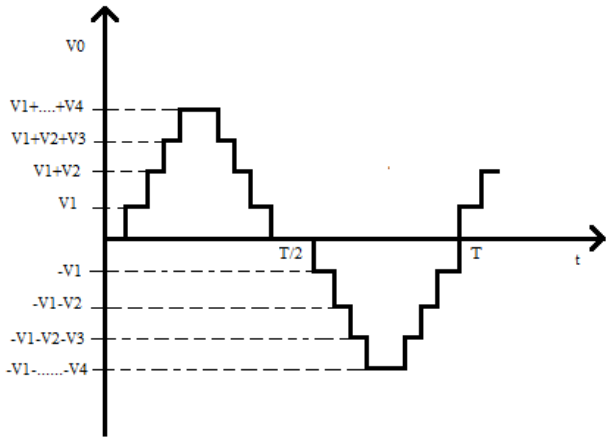

Fig. 1(b): Typical Output Waveform of V_o

The cascaded connection of these sub multilevel converters increases the possible value of V_o, effectively. But, it can only generate the positive output voltages. To generate both positive and negative voltages, a full-bridge converter is connected to the output terminal of the cascaded connection of sub multilevel converters. But, the unidirectional switches in the full-bridge converter and some bidirectional switches, such as S1, must operate at the high output voltage and need higher voltage blocking. As a result, the cost and losses will be increased and its industrial applications will be limited.

"Fig. 2" shows the proposed topology for a sub multilevel converter, hereafter called multilevel module (MLM), which is used for the implementation of the proposed multilevel converter topology. It consists of n dc voltage sources and n bidirectional switches. A MLM produces a staircase voltage waveform with positive polarity. It is connected to a single phase full-bridge converter, which particularly alternates the input voltage polarity and provides positive or negative staircase waveform at the output. The full-bridge converter has four unidirectional switches, which consists of an IGBT and an anti parallel fast recovery diode. It is noticeable that only one switch turns on in different operation modes of the MLM and also, both switches T1 and T4 (or T2 and T3) cannot be simultaneously turned on (expect state 1 in Table I) because of a short circuit occurrence across dc voltage sources and then the voltage V_o would be produced. Table I summarizes the values of the output voltage of a MLM and corresponding full-bridge converter for different state of switches S1, S2, . . . , Sn, T1, . . . , T4. State conditions 1 and 0 means that the switch is on and off respectively. For simplicity, the on state voltage drops of switches have been neglected. As it can be seen, 2n + 1 different value can be obtained for V_o.

TABLE I: VALUES OF THE OUTPUT VOLTAGE OF MLM

State	Switching States								Vo
	S1	S2	....	Sn	T1	T2	T3	T4	
1	0	0	....	0	1	0	1	0	0
	0	0	....	0	0	1	0	1	
2	1	0	....	0	0	0	1	1	V1
3	1	0	....	0	1	1	0	0	-V1
4	0	1	....	0	0	0	1	1	V1+V2
5	0	1	....	0	1	1	0	0	-V1-V2
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
2n	0	0	...	1	0	0	1	1	? v,
2n+1	0	0		1	1	1	0	0	-? vi

3. Improved Version of Proposed Technology

The proposed multilevel converter topology, which is based on the combination of MLMs and full-bridges converters, is shown in "Fig. 2". The structure of the first till k^{th} MLM has n1, n2, . . . , nk bidirectional switches, respectively. Each MLM can generate a stepped voltage waveform with positive polarity. The full-bridge converters provide positive and negative stepped voltage waveforms in their output.

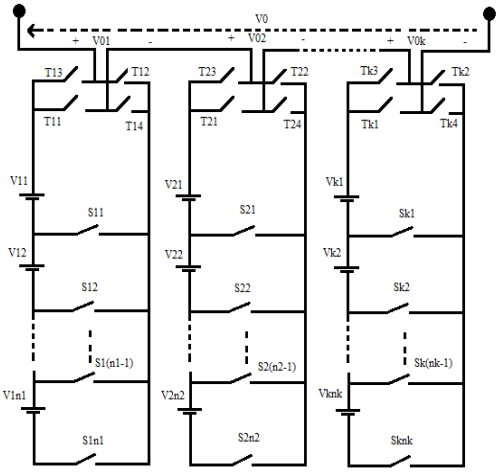

Fig. 2: Improved Version of Proposed Multilevel Inverter

The different output voltage levels can be determined by the combination of switching states of MLMs. It is obvious that only one switch of each MLM turns on in different operation modes of the converter without considering the zero voltage state of MLMs.

It should be noted that the capacitors can be replaced with the dc voltage sources in the proposed topology. Although this topology requires multiple dc voltage

sources, but they may be available in some systems through renewable energy sources, such as photovoltaic panels or fuel cells, or with energy storage devices, such as capacitors or batteries. When ac voltage is already available, then, multiple dc sources can be generated using isolated transformers and rectifiers, too [12].

If the dc voltage sources are considered to be equal in MLMs, the structure of the proposed topology will be symmetrical. In the asymmetrical structure of the proposed topology, similar to the asymmetrical cascaded multilevel converter, there is only one switching state for each output voltage level (except the zero level) to produce unequal values for v_o. In this paper, to reduce the number of components, the asymmetrical structure has been studied. It is noticeable that the asymmetrical structure has circulating energy problems. Therefore, if diode-based rectifiers are used for dc voltage sources, their dc-link voltages can increase their values dangerously.

Considering the first dc voltage source (V_{11}) as the base value of the per-unit system, i.e.,

$$V_{base} = V_{11} + V_{dc} \quad (1)$$

Then, the normalized values of the dc voltage sources for producing all levels (odd and even) in the output must be chosen using the following algorithm.

For module 1

$$V_{11} = V_{dc} \quad (2)$$

$$V_{1i} = V_{11} + V_{dc}, i = 2,...,n1 \quad (3)$$

$$V_{21} = V_{11} + 2\sum_{i=1}^{n1} V_{1i} = (2n_1 - 1)V_{dc} \quad (4)$$

$$V_{2i} = V_{21} = (2n_1 + 1)V_{dc}, i = 2,...,n2 \quad (5)$$

$$N_{level} = \sum_{i=1}^{k}(2n_i + 1) = (2n_1 + 1)x(2n_2 + 1)x...x(2n_k + 1) \quad (6)$$

4. Control Strategies

4.1 SHPWM Strategy

Instead of, maintaining the width of all pulses of same as in case of multiple pulse width modulation, the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the centre of the same pulse. The distortion factor and lower order harmonics are reduced significantly. The gating signals are generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency F_c. The frequency of reference signal F_r, determines the inverter output frequency and its peak amplitude A_r, controls the modulation index M, and rms output voltage V_0. The number of pulses per half cycle depends on carrier frequency.

4.2 ISPWM Strategy

This method provides an enhanced fundamental voltage, lower total harmonic distortion (THD) and minimizes the switch utilization among the various levels in inverters. In this method the control signals have been generated by comparing sinusoidal reference signal with a high frequency inverted sine carrier. The carrier frequencies are so selected that the number of switching in each band are equal. The proposed modulation technique maximizes the output voltage and gives a low THD.

4.3 MSPWM Strategy

This technique involves comparing several absolute sinusoidal modulation signals with single triangular carrier. This carrier signal is a train of triangular waves with frequency f_c and amplitude A_c. The single phase multilevel inverter is modeled in SIMULINK in the software package MATLAB 10. Switching signals for inverter are developed using the above mentioned PWM techniques. “Fig.3” and “Fig.4 “shows the Output voltage waveform and FFT analysis using SHPWM technique with fixed frequency for the proposed inverter (5 levels).

“Fig. 5” and “Fig. 6” shows the Output voltage waveform and FFT analysis using SHPWM technique with variable frequency.

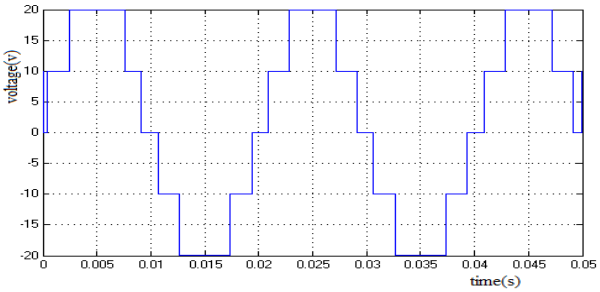

Fig. 3: Output Voltage Waveform Using SHPWM Technique with Fixed Frequency (SHPWM)

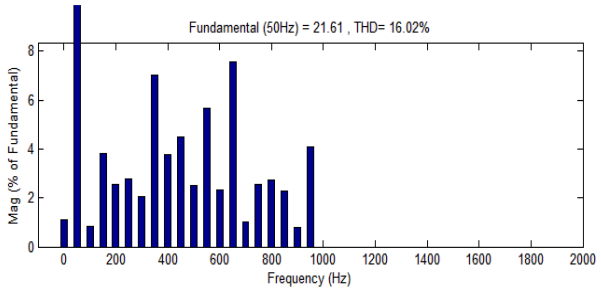

Fig. 4: FFT Analysis Using SHPWM Technique with Fixed Frequency

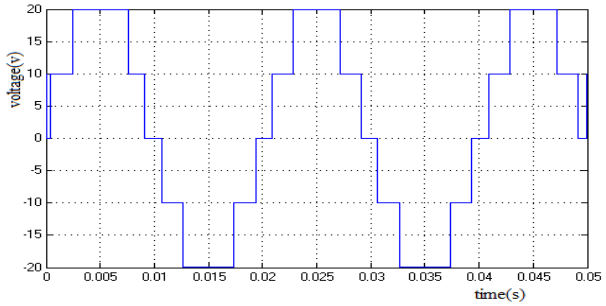

Fig. 5: Output Voltage Waveform Using SHPWM Technique with Variable Frequency (SHPWM)

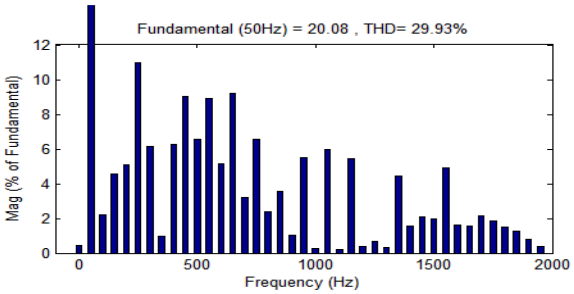

Fig. 6: FFT Analysis Using SHPWM Technique with Variable Frequency

"Fig. 7" and "Fig. 8" shows the Output voltage waveform and FFT analysis using ISPWM technique with fixed frequency for the proposed inverter (5 levels).

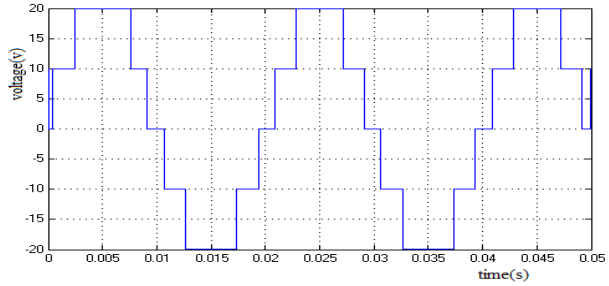

Fig. 7: Output Voltage Waveform Using ISPWM Technique with Fixed Frequency

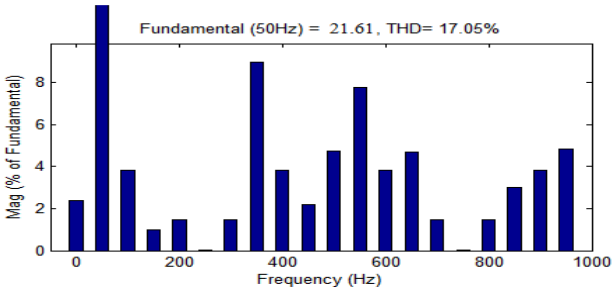

Fig. 8: FFT Analysis Using ISPWM Technique with Fixed Frequency

"Fig. 9" and "Fig. 10", the Output voltage waveform and FFT analysis using ISPWM technique with variable frequency.

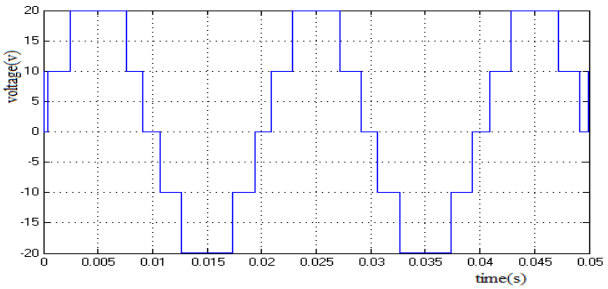

Fig. 9: Output Voltage Waveform Using ISPWM Technique with Variable Frequency

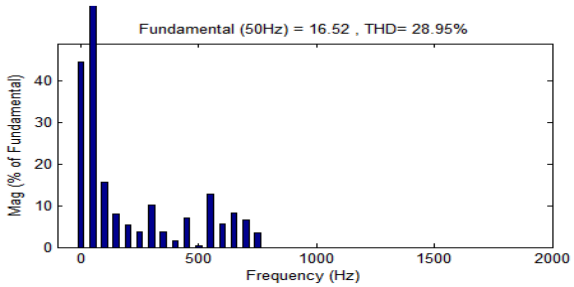

Fig. 10: FFT Analysis Using ISPWM Technique with Variable Frequency

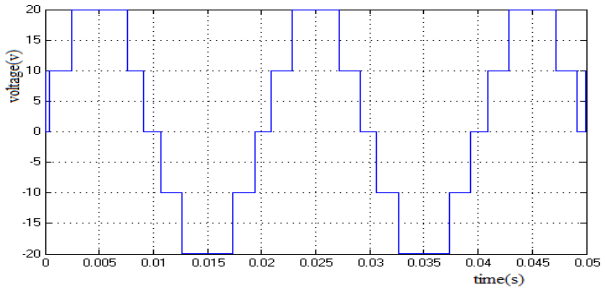

Fig. 11: Output Voltage Waveform Using MSPWM Technique with Fixed Frequency

"Fig.11" shows the Output Voltage Waveform Using MSPWM Technique. "Fig.12" shows the FFT Analysis Using MSPWM Technique.

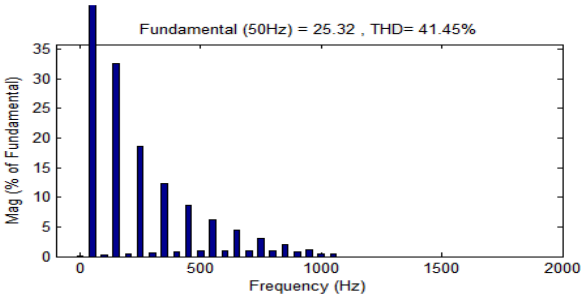

Fig. 12: FFT Analysis Using MSPWM Technique with Fixed Frequency

TABLE II: COMPARISON OF BASIC UNIT

Techniques	THD	DC Sources	No. of switches	No. of levels	Output voltage (V)
SHPWM-fixed frequency	16.02 %	2	8	5	21.61
SHPWM-variable frequency	29.93 %	2	8	5	20.08
ISPWM-fixed frequency	17.05 %	2	8	5	21.61
ISPWM-variable frequency	28.95 %	2	8	5	16.52
MSPWM	41.45 %	2	8	5	25.32

From the Table II, the SHPWM with fixed frequency has less total harmonic distortion. "Fig.13" shows the Output Voltage Waveform Using SHPWM Technique with Fixed Frequency for improved version (25 levels). "Fig.14" shows the FFT Analysis Using SHPWM Technique with Fixed Frequency.

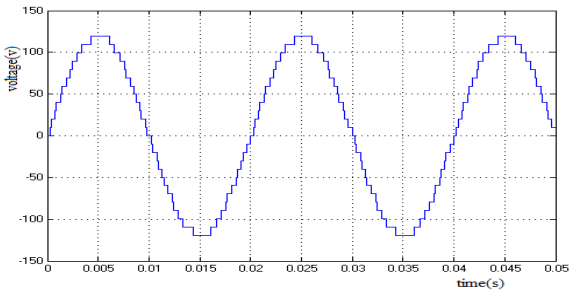

Fig. 13: Output Voltage Waveform Using SHPWM Technique with Fixed Frequency

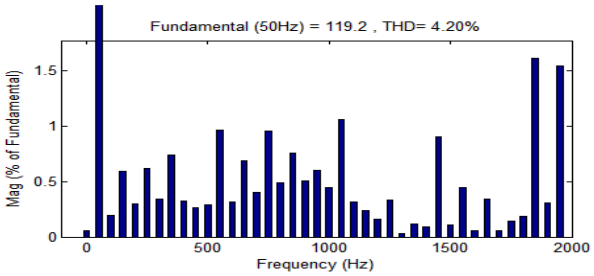

Fig. 14: FFT Analysis Using SHPWM Technique with Fixed Frequency

"Fig. 15" shows the Output voltage waveform and FFT analysis using SHPWM technique with variable frequency for the improved inverter (25 levels). "Fig. 16" shows the FFT analysis using SHPWM technique with variable frequency.

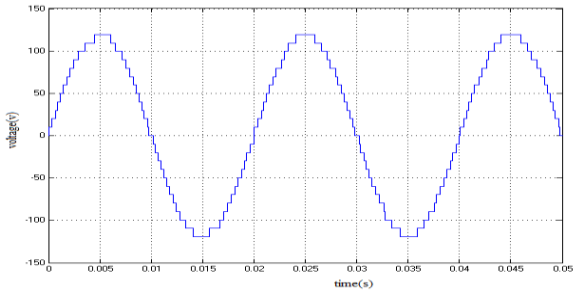

Fig. 15: Output Voltage Waveform Using SHPWM Technique with variable frequency

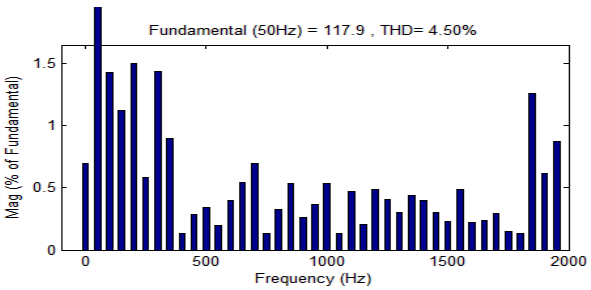

Fig. 16: FFT Analysis Using SHPWM Technique with variable Frequency

"Fig. 17" and "Fig. 18" shows the Output voltage waveform and FFT analysis using ISPWM technique with fixed frequency for the improved inverter (25 levels).

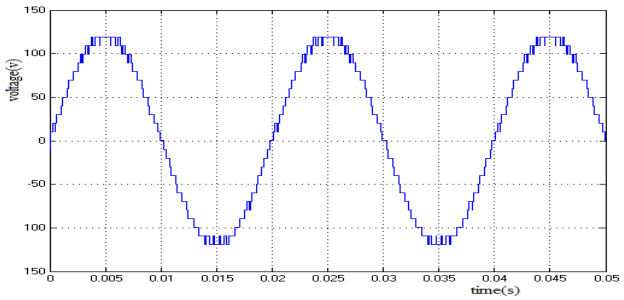

Fig. 17: Output Voltage Waveform Using ISPWM Technique with Fixed Frequency

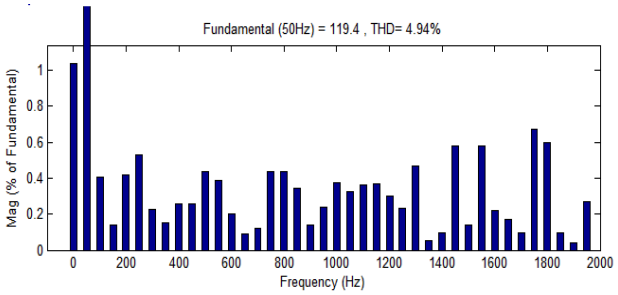

Fig. 18: FFT Analysis Using ISPWM Technique with Fixed Frequency

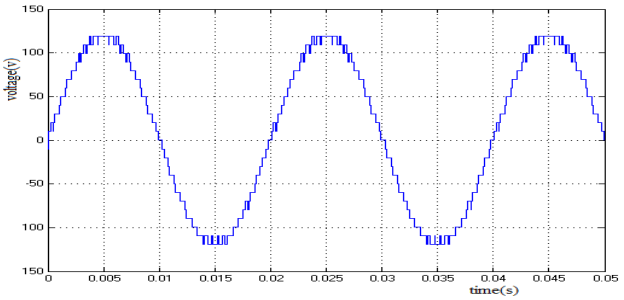

Fig. 19: Output Voltage Waveform Using ISPWM Technique with variable Frequency

'Fig. 19" and "Fig. 20" Shows the Output voltage waveform and FFT analysis using ISPWM technique with variable frequency for the improved inverter (25 levels).

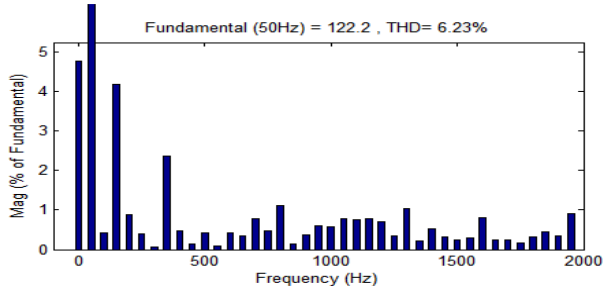

Fig. 20: FFT Analysis Using ISPWM Technique with variable Frequency

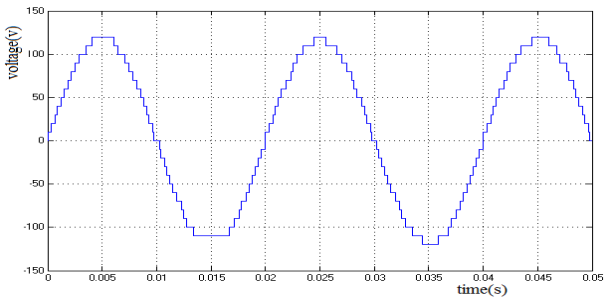

Fig. 21: Output Voltage Waveform Using MSPWM Technique

"Fig. 21" and "Fig. 22" Shows the Output voltage waveform and FFT analysis using MSPWM technique for the improved inverter (25 levels).

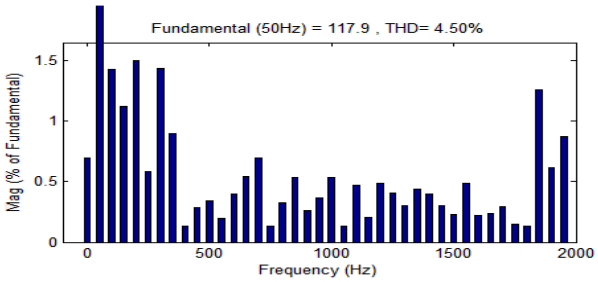

Fig. 22: FFT Analysis Using MSPWM Technique

From the Table II, the SHPWM with fixed frequency has less total harmonic distortion.

TABLE II: COMPARISON OF IMPROVED VERSION

Techniques	THD	DC Sources	No. of switches	No. of levels	Output voltage (V)
SHPWM-fixed frequency	4.20%	4	16	25	119.2
SHPWM-variable frequency	4.50%	4	16	25	117.9
ISPWM-fixed frequency	4.94%	4	16	25	119.4
ISPWM-variable frequency	6.23%	4	16	25	122.2
MSPWM	4.50%	4	16	25	117.8

From the Tables I and II, the THD values of the SHPWM, ISPWM and MSPWM are tabulated for 5-levels and 25-levels. It can be seen that SHPWM technique yields a better performance than other techniques.

5. Dynamic voltage restorer

DVR is a power electronic based device that injects

voltage into the system to regulate the load side voltage [17],[18]. It is normally installed between supply and critical load feeder. The basic function of DVR is to boost up the load side voltage in the event of disturbance in order to avoid any power disruption to the load. There are many control technique available to implement the DVR. The primary function of DVR is to compensate voltage sags and swells but it can also perform the tasks such as: harmonic compensation, reduction of transient in voltage and fault current limitation.

The main parts of DVR are:

- injection transformer,
- harmonic filter,
- a voltage source converter,
- energy storage device
- control & protection system

The components are divided into three major model components: supply, dynamic voltage restorer and load. The detailed model description of Dynamic Voltage Restorer is presented in following paragraphs of software development

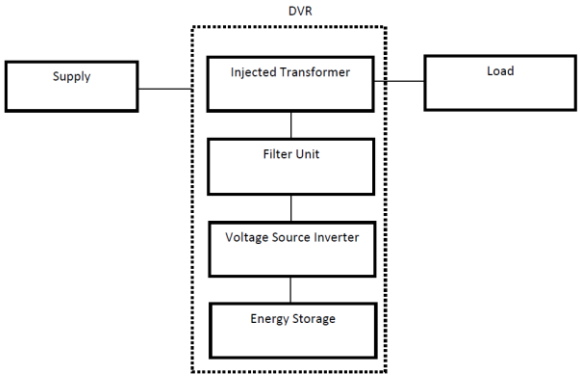

Fig. 23: Block diagram of DVR

The block diagram of DVR for voltage compensation is shown in "Fig. 23". Dynamic voltage restorer [19] is a series connected device is used for mitigating voltage disturbances in the distribution system. Voltage sags caused by unsymmetrical line-to line, line to ground, double-line-to-ground and symmetrical three phase faults is affected to sensitive loads.

Consider a three phase power system with base voltage - 100V, Frequency - 50 Hz, MVA rating-100MVA. Due to voltage sag in power system the output voltage and current are disturbed between 0.4-0.5s**.** **"**Fig. 24" and "Fig. 25" shows the voltage and current waveforms.

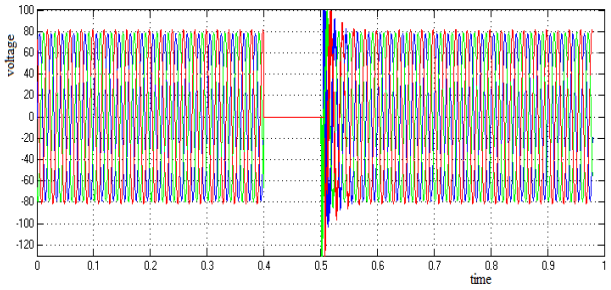

Fig. 24: Output Voltage Waveform For Voltage Sag

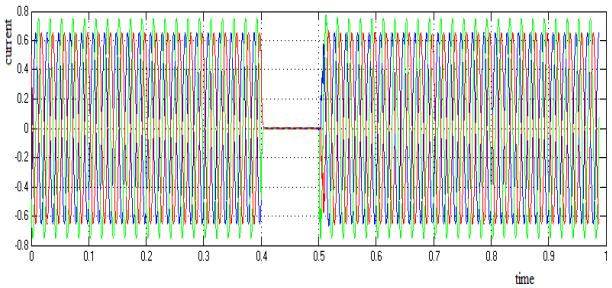

Fig. 25: Output current Waveform For Voltage Sag

The DVR injects the independent voltages to restore and maintained sensitive to its nominal value. Then the voltage sag can be compensated by DVR. "Fig. 26" and "Fig. 27" shows the voltage and current waveforms after compensation.

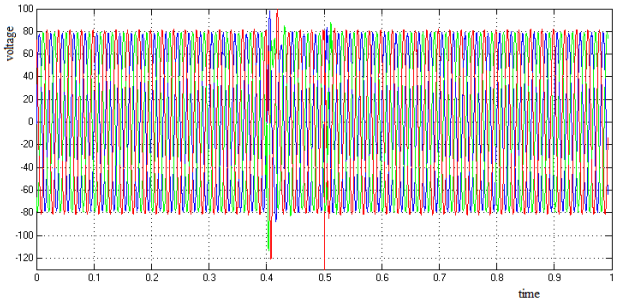

Fig. 26: Output Voltage Waveform With DVR

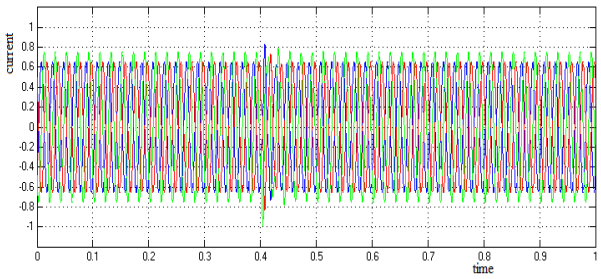

Fig. 27: Output Current Waveform With DVR

6. Conclusion

A new basic multilevel module has been proposed. The proposed topology and improved version of proposed topology is analysed and simulated for 5 levels and 25 levels with three different control techniques. The main achievement of this control techniques are the reduction in their total harmonic distortion (THD), closer to sinusoidal waveform without the usage of an output filter. Proposed multilevel inverter reduces the switching losses by reducing number of switches and provides improved output voltage capability. It can be observed that SHPWM produces a better fundamental output voltage and minimized total harmonic distortion (THD). The proposed topologies can be a good solution for applications that require high power quality. The improved version of proposed multilevel inverter has reduced THD and higher output voltage with reduced number of switches. So this configuration is used as a DVR in power system for voltage sag compensations. In case of voltage sag in power system, DVR injects the voltage which is in phase with the supply voltage. The load side connected converter topology has capability of mitigating the long duration voltage sags on the line. Simulation of DVR has been developed by using Matlab/Simulink. The simulation results show that the DVR compensates the sag quickly and provides excellent voltage regulation.

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