

Design and Implementation of 15-Level Asymmetric Cascaded H Bridge Multilevel Inverter

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Abstract—This paper presents a Design and Implementation of 15-Level Asymmetrical Cascaded H Bridge Multilevel Inverter. In this system Symmetrical and Asymmetrical Multilevel inverter (MLI) is utilized. In Symmetrical MLI, the DC source magnitude's are equal i.e., $60V_{dc}$, $60V_{dc}$, $60V_{dc}$ & $60V_{dc}$, where as in Asymmetrical MLI the DC source Magnitude's are unequal and it is designed with binary form of voltage such as $33V_{dc}$, $66V_{dc}$ & $132V_{dc}$. Comparing both the MLI, Asymmetrical MLI generates a number of output voltage level with same number of Power semiconductor switches. The phase Disposition Pulse Width Modulation (PD-PWM) technique is used for controlling the Power semiconductor switches in MLI. The results are verified in MATLAB, PROTEUS and real time system

Keywords—Photo voltaic system(PV), Symmetrical MLI, Asymmetrical MLI, PD-PWM, PIC16F877A, IR112.

I. INTRODUCTION

In recent years, countries all over the world has its attention towards global warming. One of the cause is conventional fossil fuel based power generating sources and it has become a serious concern. Among the usage of renewable energy resources like wind, solar, geothermal etc., photovoltaic (PV) system is very important source of energy and it has acquired a lot of attention due to the research and development in the fabrication of solar cell. Power electronic converter technology is required for generation of solar power, which reduces the cost and enhances the system efficiency.

Multilevel Inverter (MLI) has more advantages than conventional inverter because of less switching losses, less voltage stress across switch and less Electromagnetic Interference (EMI). Generally there are three basic types of MLI they are Neutral point Clamped (NPC MLI), Flying Capacitor (FC MLI) and Cascaded H-Bridge (CHB MLI). The Figure 1 shows the classification of MLI. NPCMLI consists of clamping diodes which increases the voltage levels. The capacitor is connected in series for voltage balancing. This makes a huge problem for devices. In FCMLI more number of clamping capacitors are connected, so the voltage balancing is difficult. CHBMLI is suitable for high voltage applications because, each H bridge consists of 4 switches and one DC source. Clamping capacitors and diodes are not used here[1]-[5]. In CHBMLI Topology, depending upon DC source it consists of two types, 1. Single DC source and 2. Multiple DC source. In Single DC source the CHBMLI is

connected in parallel and to the output of each H Bridge is connected to the low frequency transformer is Primary side. Whereas secondary side transformer is connected in series across the load. To increase the "n" number of levels the Transformer is increased for each H Bridge inverter, so that the efficiency of system will become less. In multiple DC Source the CHBMLI is connected in series. To increase the "n" number of output voltage levels the several H-Bridge and DC source are used. To reduce the switches in this topology the Symmetrical and Asymmetrical CHBMLI are utilized.[2]

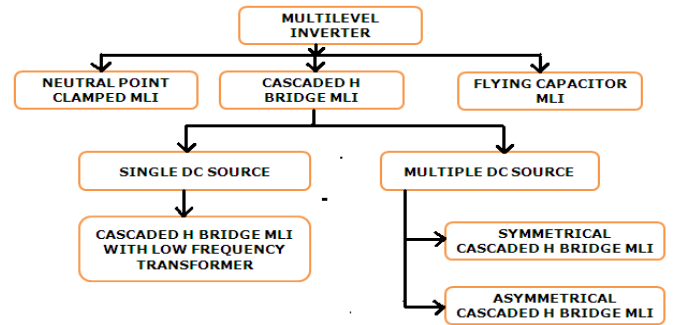


Fig. 1. Classifications of Multilevel Inverter

A. Symmetrical Cascaded H Bridge Multilevel Inverter

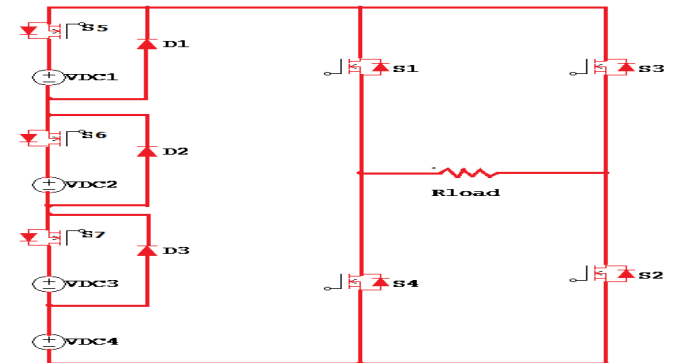


Fig. 2. Symmetrical multilevel inverter

Figure 2 represents the Symmetrical Cascaded H Bridge Inverter (SCHB-MLI) topology. In this circuit, when MOSFET Controlled Switch is Turned On, the DC Voltage Source and MOSFET Controlled Switch are connected in series, so that the current flows from DC Source to MOSFET

and the Diode becomes Reverse biased Condition. When MOSFET controlled Switch is turned OFF , the Current flows via diode and the diode is forward biased.The Circuit needs four DC voltage sources,7 switches and 3 diodes. The 4 DC sources are equal with Voltage of $60V_{DC}$, and this circuit will generate Nine Level output voltage of $240V_{DC}$, $180V_{DC}$, $120V_{DC}$, $60V_{DC}$, $0V_{DC}$, $-60V_{DC}$, $-120V_{DC}$, $-180V_{DC}$, $-240V_{DC}$ respectively.[2]

TABLE I. THE SWITCHING CONFIGURATION OF SYMMETRICAL CHBMLI

V_o	S1	S2	S3	S4	S5	S6	S7
V_{dc}	ON	ON	OFF	OFF	ON	ON	ON
$3V_{dc}/4$	ON	ON	OFF	OFF	OFF	ON	ON
$2V_{dc}/4$	ON	ON	OFF	OFF	OFF	OFF	ON
$V_{dc}/4$	ON	ON	OFF	OFF	OFF	OFF	OFF
0	OFF	ON	ON	OFF	OFF	OFF	OFF
$V_{dc}/4$	OFF	OFF	ON	ON	OFF	OFF	OFF
$2V_{dc}/4$	OFF	OFF	ON	ON	OFF	OFF	ON
$3V_{dc}/4$	OFF	OFF	ON	ON	OFF	ON	ON
V_{dc}	OFF	OFF	ON	ON	ON	ON	ON

In SCHBMLI the total Number of switches and the output voltage levels are obtained as follows

$$N_{level}=2n+3 \quad (1)$$

$$N_{MOSFET}=n+4 \quad (2)$$

The 'n' Represents the number of MOSFET in Symmetrical unit Circuit.

B. Asymmetrical Cascaded H Bridge Multilevel Inverter

Figure 3 represents the Asymmetrical Cascaded H Bridge Inverter (ASCHB-MLI) topology. In this Inverter the DC source magnitudes are unequal. The DC source magnitude are designed with binary form of voltage such as $25V_{DC}$, $50V_{DC}$, $100V_{DC}$ respectively. Both the inverter consists of same number of Power semiconductor switches but the voltage level varies. In SCHBMLI the output voltage is 9level, where as in ASCHBMLI the output voltage is 15 level and they are $33V_{dc}$, $66V_{dc}$, $99V_{dc}$, $132V_{dc}$, $165V_{dc}$, $198V_{dc}$, $231V_{dc}$, $0V_{dc}$, $-33V_{dc}$, $-66V_{dc}$, $-99V_{dc}$, $-132V_{dc}$, $-165V_{dc}$, $-198V_{dc}$, $-231V_{dc}$ respectively.[3]-[4]

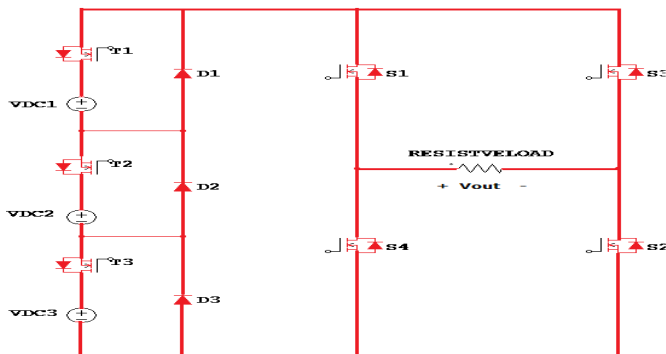


Fig. 3. Asymmetrical multilevel inverter

In ASCHMLI the number of switches and number of levels are represented as follows[6]-[7]

$$N_{level}=2^{(n+1)}-1 \quad (3)$$

$$N_{MOSFET}=n+4 \quad (4)$$

II. SWITCHING MODE OF OPERATION FOR 15 LEVEL PROPOSED INVERTER

A. Mode1:Maximum Positive output Voltage (V_{dc})

When MOSFET Switches S_1, S_2, S_3 & S_4 are turned ON, the maximum positive voltage V_{dc} is united to the (+ve) terminal (a) of the load. When the MOSFET Switch S_5 is turned ON , the (-ve) terminal (b) of the load is connected to the ground and remaining all the switches are in OFF condition. The current flows through the load from 'a' to 'b', so that the voltage brought to bear across the load is $+V_{dc}$ as shown in figure 4.

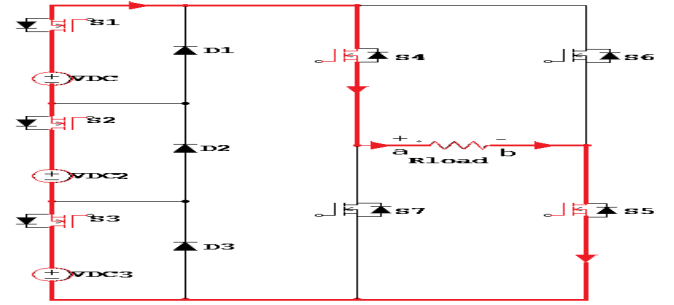


Fig. 4. Output Voltage level $V_{ab}=V_{dc}$ to generate the Switching Sequence.

B. Mode 2: Positive output voltage ($6V_{dc}/7$):

When MOSFET Switches S_2, S_3 & S_4 are turned ON and MOSFET Switch S_1 is turned OFF the current flows via Diode D_1 , So that the positive voltage $6V_{dc}/7$ is united to the (+ve) terminal (a) of the load. When the MOSFET Switch S_5 is turned ON , the (-ve) terminal (b) of the load is united to the ground and remaining all the switches are in OFF condition. The current flows through the load from 'a' to 'b', so that the voltage brought to bear across the load is $+6V_{dc}/7$ as shown in figure 5.

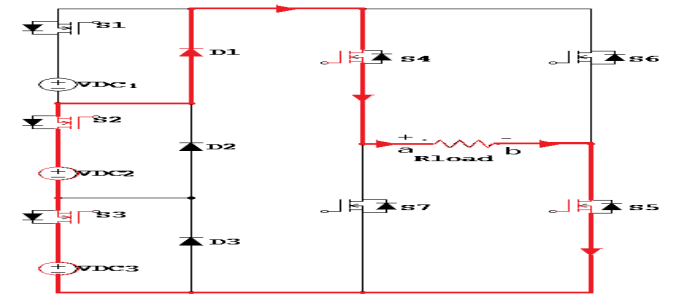


Fig. 5. Output Voltage level $V_{ab} = 6V_{dc}/7$ to generate the Switching Sequence

C. Mode 3: Positive output voltage ($5V_{dc}/7$):

When MOSFET Switches S_1, S_3 & S_4 are turned ON and MOSFET Switch S_2 is turned OFF the current flows via

Diode D_2 So that the positive voltage $5V_{dc}/7$ is united to the (+ve) terminal (a) of the load. When the MOSFET S_5 is turned ON, the (-ve) terminal (b) of the load is united to the ground and remaining all the switches are in OFF condition. The current flows through the load from 'a' to 'b', so that the voltage brought to bear across the load is $+5V_{dc}/7$ as shown in figure 6.

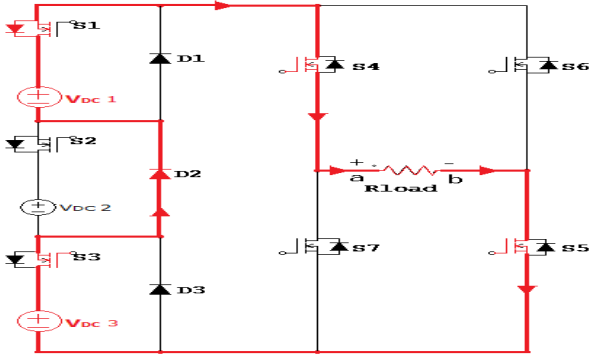


Fig. 6. Output Voltage level $V_{ab} = 5V_{dc}/7$ to generate the Switching Sequence

D. Mode 4: Positive output voltage ($4V_{dc}/7$):

When MOSFET Switches S_3 & S_4 are turned ON and MOSFET Switch S_1 & S_2 is turned OFF the current flows via Diode D_1 & D_2 . So that the positive voltage $4V_{dc}/7$ is united to the (+ve) terminal (a) of the load. When the MOSFET Switch S_5 is turned ON, the (-ve) terminal (b) of the load is united to the ground and remaining all the switches are in OFF condition. The current flows through the load from 'a' to 'b', so that the voltage brought to bear across the load is $+4V_{dc}/7$ as shown in figure 7.

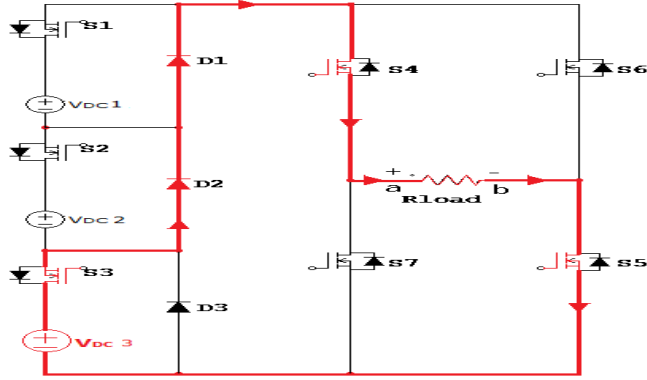


Fig. 7. Output Voltage level $V_{ab} = 4V_{dc}/7$ to generate the Switching Sequence

E. Mode 5: Positive output voltage ($3V_{dc}/7$):

When MOSFET Switches S_1, S_2 & S_4 are turned ON and MOSFET Switch S_3 is turned OFF the current flows via Diode D_3 . So that the positive voltage $3V_{dc}/7$ is united to the (+ve) terminal (a) of the load. When the MOSFET Switch S_5 is turned ON, the (-ve) terminal (b) of the load is united to the

ground and remaining all the switches are in OFF condition. The current flows through the load from 'a' to 'b', so that the voltage brought to bear across the load is $+3V_{dc}/7$ as shown in figure 8.

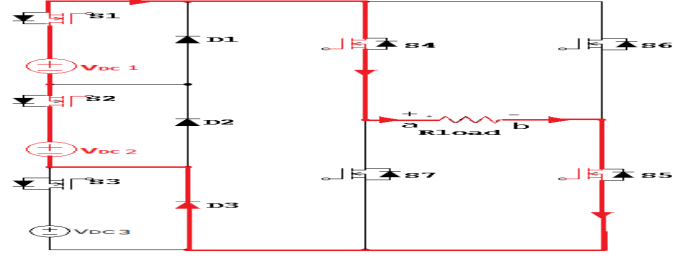


Fig. 8. Output Voltage level $V_{ab} = 3V_{dc}/7$ to generate the Switching Sequence

F. Mode 6: Positive output voltage ($2V_{dc}/7$):

When MOSFET switches S_2 & S_4 are turned ON and Switch S_1 & S_3 is turned OFF the current flows via Diode D_1 & D_3 . So that the positive voltage $2V_{dc}/7$ is united to the (+ve) terminal (a) of the load. When the MOSFET switch S_5 is turned ON, the (-ve) terminal (b) of the load is united to the ground and remaining all the switches are in OFF condition. The current flows through the load from 'a' to 'b', so that the voltage brought to bear across the load is $+2V_{dc}/7$ as shown in figure 9.

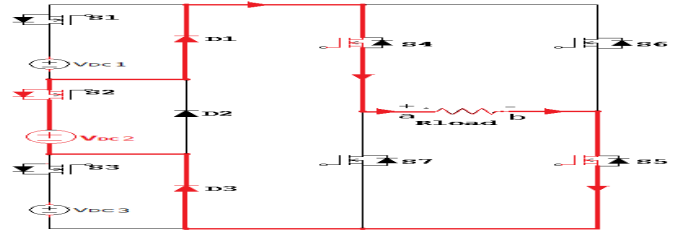


Fig. 9. Output Voltage level $V_{ab} = 2V_{dc}/7$ to generate the Switching Sequence

G. Mode 7: Positive output voltage ($V_{dc}/7$):

When MOSFET switches S_1 & S_4 are turned ON and MOSFET Switch S_2 & S_3 is turned OFF the current flows via Diode D_2 & D_3 . So that the positive voltage $1V_{dc}/7$ is united to the (+ve) terminal (a) of the load. When the MOSFET switch S_5 is turned ON, the (-ve) terminal (b) of the load is united to the ground and remaining all the switches are in OFF condition. The current flows through the load from 'a' to 'b', so that the voltage brought to bear across the load is $+1V_{dc}/7$ as shown in figure 10.

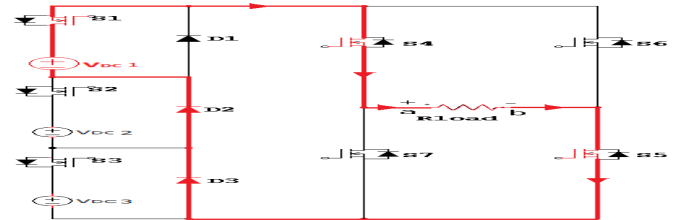


Fig. 10. Output Voltage level $V_{ab} = V_{dc}/7$ to generate the Switching Sequence

H. Mode 8: Zero output voltage ($0V_{dc}$):

The Zero Output voltage level is produced by turning ON MOSFET Switches S_7 & S_5 or S_4 & S_6 and remaining controlled switches are in off condition. When MOSFET switches S_7 & S_5 or S_4 & S_6 are turned on, the output voltage across the load is zero as shown in the figure 11

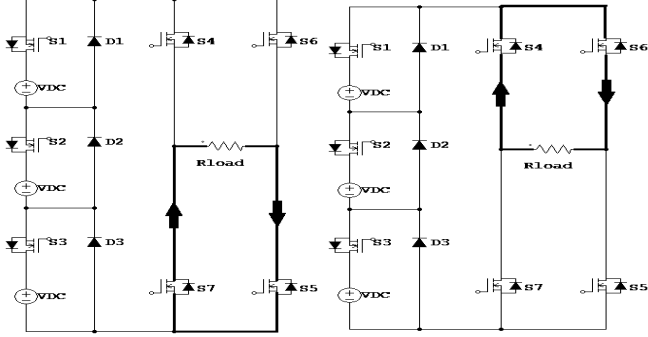


Fig. 11. Output Voltage level $V_{ab} = 0V_{dc}$ to generate the Switching Sequence

I. Mode 9: Negative Output voltage ($-1V_{dc}/7$):

When MOSFET Switches S_1 & S_6 are turned ON and MOSFET Switch S_2 & S_3 is turned OFF the Current flows via Diode D_2 & D_3 , So that the Positive voltage $V_{dc}/7$ is united to the (-ve) terminal (b) of the load. When the MOSFET switch S_7 is turned ON, the (+ve) terminal (a) of the load is united to the ground and remaining all the switches are in OFF condition. The current flows through the load from 'b' to 'a', so that the voltage brought to bear across the load is $-1V_{dc}/7$ as shown in figure 12.

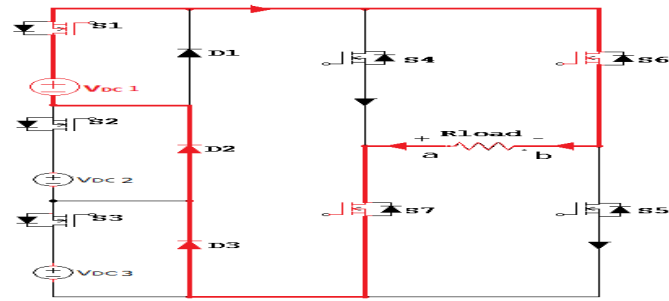


Fig. 12. Output Voltage level $V_{ab} = -V_{dc}/7$ to generate the Switching Sequence

J. Mode 10: Negative Output voltage ($-2V_{dc}/7$):

When MOSFET switches S_2 & S_6 are turned ON and MOSFET Switch S_1 & S_3 is turned OFF the Current flows via Diode D_1 & D_3 , So that the Positive voltage $2V_{dc}/7$ is united to the (-ve) terminal (b) of the load. When the MOSFET switch S_7 is turned ON, the (+ve) terminal (a) of the load is united to the ground and remaining all the switches are in OFF condition. The current flows through the load from 'b' to 'a', so that the voltage brought to bear across the load is $-2V_{dc}/7$ as shown in figure 13.

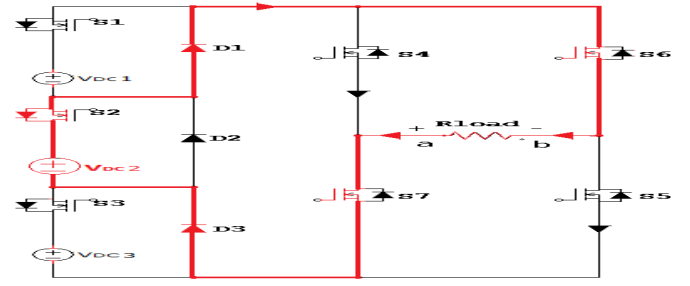


Fig. 13. Output Voltage level $V_{ab} = -2V_{dc}/7$ to generate the Switching Sequence

K. Mode 11: Negative Output voltage ($-3V_{dc}/7$):

When MOSFET Switches S_1 , S_2 & S_6 are turned ON and MOSFET Switch S_3 is turned OFF the Current flows via Diode D_3 , So that the Positive voltage $3V_{dc}/7$ is united to the (-ve) terminal (b) of the load. When the MOSFET S_7 is turned ON, the (+ve) terminal (a) of the load is united to the ground and remaining all the switches are in OFF condition. The current flows through the load from 'b' to 'a', so that the voltage brought to bear across the load is $-3V_{dc}/7$ as shown in figure 14.

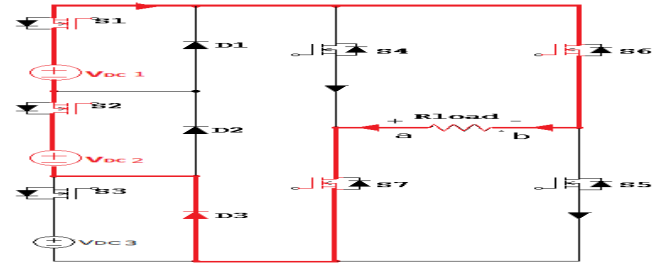


Fig. 14. Output Voltage level $V_{ab} = -3V_{dc}/7$ to generate the Switching Sequence

L. Mode 12: Negative Output voltage ($-4V_{dc}/7$):

When MOSFET Switches S_3 & S_6 are turned ON and MOSFET Switches S_1 & S_2 are turned OFF the Current flows via Diode D_1 & D_2 , So that the Positive voltage $4V_{dc}/7$ is united to the (-ve) terminal (b) of the load. When the MOSFET switch S_7 is turned ON, the (+ve) terminal (a) of the load is united to the ground and remaining all the switches are in OFF condition. The current flows through the load from 'b' to 'a', so that the voltage brought to bear across the load is $-4V_{dc}/7$ as shown in figure 15

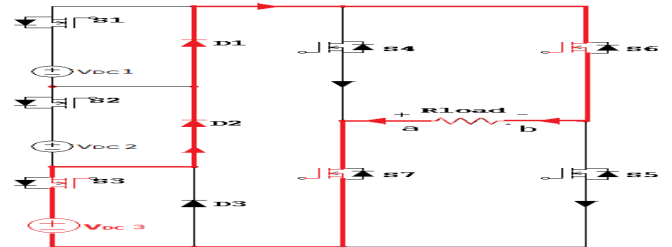


Fig. 15. Output Voltage level $V_{ab} = -4V_{dc}/7$ to generate the Switching Sequence

M. Mode 13: Negative Output voltage($-5V_{dc}/7$):

When MOSFET switches S_1, S_3 & S_6 are turned ON and MOSFET Switch S_2 is turned OFF the Current flows via Diode D_2 , So that the Positive voltage $5V_{dc}/7$ is united to the (-ve) terminal (b) of the load. When MOSFET switch S_7 is turned ON, the (+ve) terminal (a) of the load is united to the ground, remaining all the switches are in OFF condition. The current flows through the load from 'b' to 'a', so that the voltage brought to bear across the load is $-5V_{dc}/7$ as shown in figure 16.

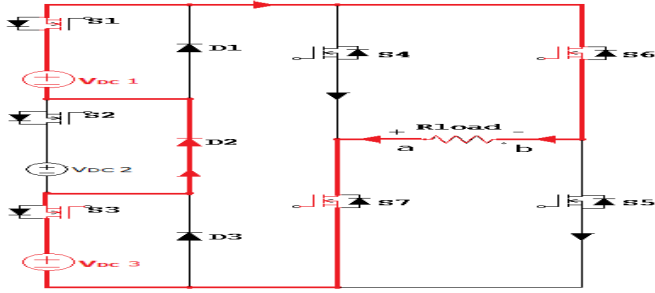


Fig. 16. Output Voltage level $V_{ab} = -5V_{dc}/7$ to generate the Switching Sequence

N. Mode 14: Negative Output voltage($-6V_{dc}/7$):

When MOSFET Switches S_2, S_3 & S_6 are turned ON and MOSFET Switch S_1 is turned OFF the Current flows via Diode D_1 , So that the Positive voltage $6V_{dc}/7$ is united to the (-ve) terminal (b) of the load. When the MOSFET switch S_7 is turned ON, the (+ve) terminal (a) of the load is united to the ground and remaining all the switches are in OFF condition. The current flows through the load from 'b' to 'a', so that the voltage brought to bear across the load is $-6V_{dc}/7$ as shown in figure 17.

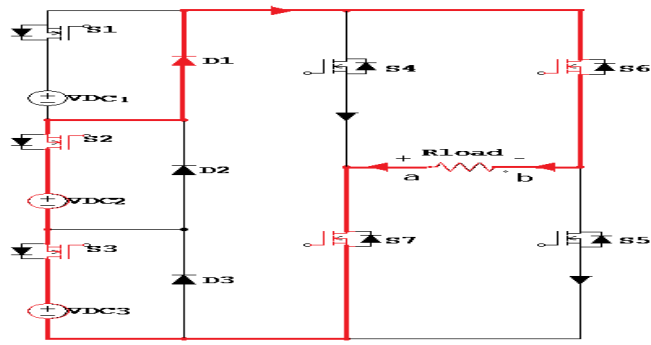


Fig. 17. Output Voltage level $V_{ab} = -6V_{dc}/7$ to generate the Switching Sequence

O. Mode 15: Negative Output voltage($-V_{dc}$):

When MOSFET Switches S_1, S_2, S_3 & S_6 are turned ON, the Positive voltage $V_{dc}/7$ is united to the (-ve) terminal (b) of the load. When the MOSFET switch S_7 is turned ON, the (+ve) terminal (a) of the load is united to the ground and remaining all the switches are in OFF condition. The current flows through the load from 'b' to 'a', so that the voltage brought to bear across the load is $-V_{dc}$ as shown in figure 18.

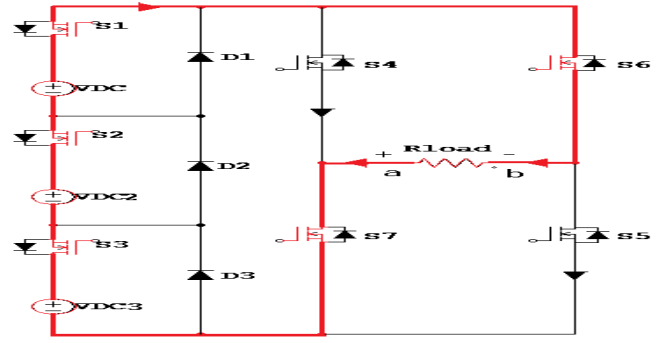


Fig. 18. Output Voltage level $V_{ab} = -V_{dc}$ to generate the Switching Sequence

TABLE II. OUTPUT VOLTAGE ACCORDING TO THE SWITCHING ON-OFF CONDITION

V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7
V_{dc}	1	1	1	1	1	0	0
$6V_{dc}/7$	0	1	1	1	1	0	0
$5V_{dc}/7$	1	0	1	1	1	0	0
$4V_{dc}/7$	0	0	1	1	1	0	0
$3V_{dc}/7$	1	1	0	1	1	0	0
$2V_{dc}/7$	0	1	0	1	1	0	0
$V_{dc}/7$	1	0	0	1	1	0	0
$0V_{dc}$	0	0	0	1	0	1	0
$0V_{dc}$	0	0	0	0	1	0	1
$-1V_{dc}/7$	1	0	0	0	0	1	1
$-2V_{dc}/7$	0	1	0	0	0	1	1
$-3V_{dc}/7$	1	1	0	0	0	1	1
$-4V_{dc}/7$	0	0	1	0	0	1	1
$-5V_{dc}/7$	1	0	1	0	0	1	1
$-6V_{dc}/7$	0	1	1	0	0	1	1
$-V_{dc}$	1	1	1	0	0	1	1

Table 2 shows the switching combination that generated the 15 level output voltage level ($0V_{dc}, V_{dc}/7, 2V_{dc}/7, 3V_{dc}/7, 4V_{dc}/7, 5V_{dc}/7, 6V_{dc}/7, V_{dc}, -V_{dc}/7, -2V_{dc}/7, -3V_{dc}/7, -4V_{dc}/7, -5V_{dc}/7, -6V_{dc}/7, -V_{dc}$)

III. PWM SWITCHING TECHNIQUE

In Figure 19 shows the Modulation Technique. The Modulation Control Scheme is divided into two types they are fundamental switching (low switching) frequency and (High switching Frequency) PWM. In this ACHMLI the Phase Disposition Pulse Width Modulation Technique (PD- PWM) is utilized with switching frequency of 2KHz. This PD-PWM technique is used to control the Switches in the inverter. Figure 20 shows the generation of PD-PWM technique for

ASCHBMLI. In this technique it consists of 14 carrier signals (2KHz) and sine wave fundamental frequency (50Hz) by using logical circuits the switching pulse are generated [7]-[8].

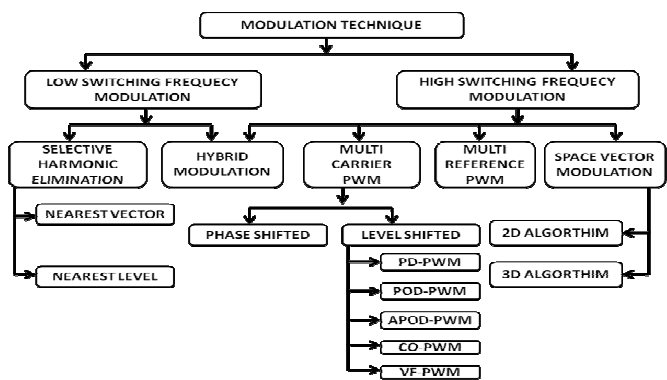


Fig. 19. Modulation Technique for Inverter

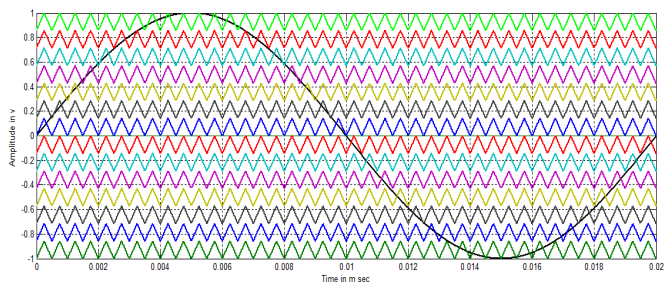


Fig. 20. PD-PWM Switching signal Generation

IV. SIMULATION AND RESULTS

Figure 21 shows the ASCHMLI with PD-PWM technique. The ASCHBMLI consists of three DC sources, seven MOSFET Controlled Switches and three Diodes.

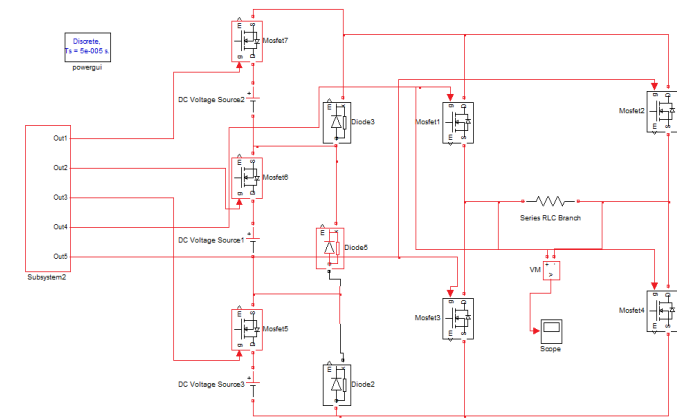


Fig. 21. A 15 level ASCHB Inverter with PD-PWM technique.

In Pulse Width Modulation(PWM) technique,the PD-PWM is used to control the MOSFET switches in the inverter

and to reduce the Total Harmonic Distortion(THD) .Figure 22,23 and 24 shows the Output PD-PWM switching for S_1 , S_2 & S_3 .The switches of S_1 , S_2 & S_3 are generated with high switching frequency of 2KHz,where as in the Cascaded H bridge Inverter (CHBI), the Switches S_4 , S_5 , S_6 & S_7 are generated with low switching frequency of 50Hz as shown in figure 25.The 15-level output voltage for ASCHBMLI with PD-PWM is shown in figure 26.The output voltage levels are $231V_{dc}$, $198V_{dc}$, $165V_{dc}$, $132V_{dc}$, $99V_{dc}$, $66 V_{dc}$, $33 V_{dc}$, $0 V_{dc}$, $-33 V_{dc}$, $-66 V_{dc}$, $-99 V_{dc}$, $-132 V_{dc}$, $-165V_{dc}$, $-198V_{dc}$, $-231V_{dc}$ respectively.Figure 27 represents the THD analysis of ASCHBML with PD-PWM.[9]

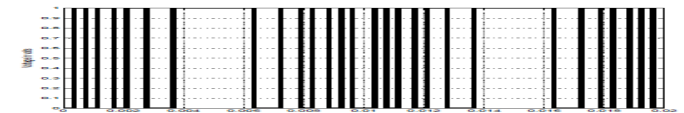


Fig. 22. PD-PWM signals for S_1

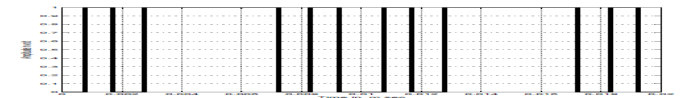


Fig. 23. PD-PWM signals for S_2

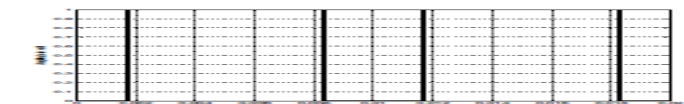


Fig. 24. PD-PWM signals for S_3

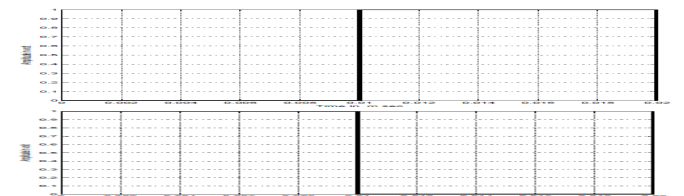


Fig. 25. PWM signals for S_4 , S_5 , S_6 & S_7

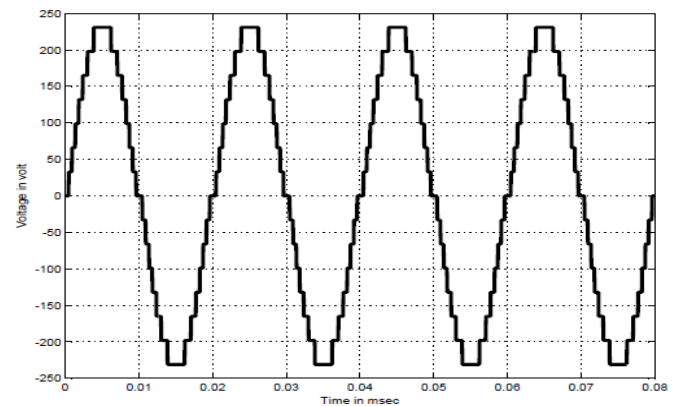


Fig. 26. Output Voltage for Asymmetric 15 level CHB Inverter

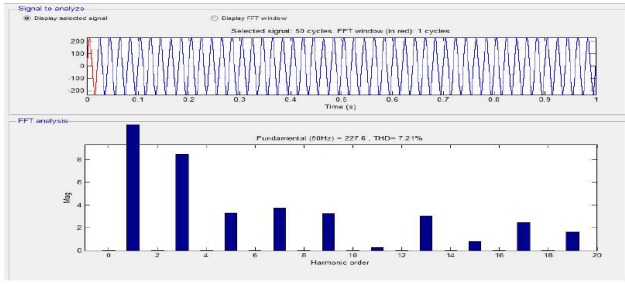


Fig. 27. THD Analysis for Asymmetric 15 level CHB Inverter using pulse

The 9-level output voltage for SCHBMLI with PD-PWM as shown in figure 28. In SCHBMLI the output voltage levels are $240V_{dc}$, $180V_{dc}$, $120V_{dc}$, $60V_{dc}$, $0V_{dc}$, $-60V_{dc}$, $-120V_{dc}$, $-180V_{dc}$, $-240V_{dc}$ respectively. In figure 29 represents the THD analysis of SCHBMLI with PD-PWM.[8]

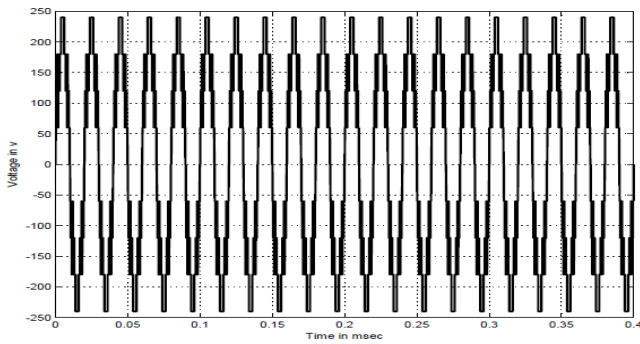


Fig. 28. Output Voltage for 9 level SCHB Inverter using PD-PWM

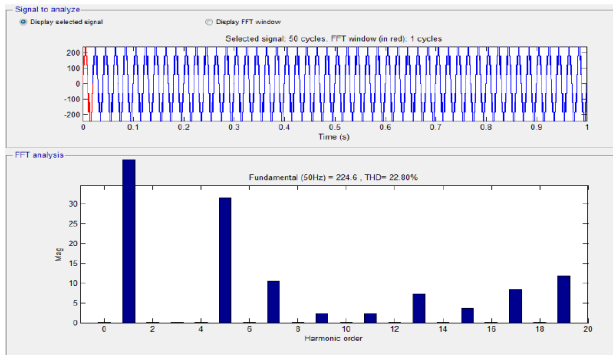


Fig. 29. THD analysis for 9-level SCHBMLI with PD-PWM

TABLE III. COMPARISON OF THD FOR SYMMETRICAL AND ASYMMETRICAL MULTILEVEL INVERTER

S.no	MLI	NUMBER OF LEVELS	THD
1	ASYMMETRICAL MLI	15-LEVEL	7.21%
2	SYMMETRICAL MLI	9-LEVEL	22.00%

V. PROTEUS SOFTWARE OUTPUT

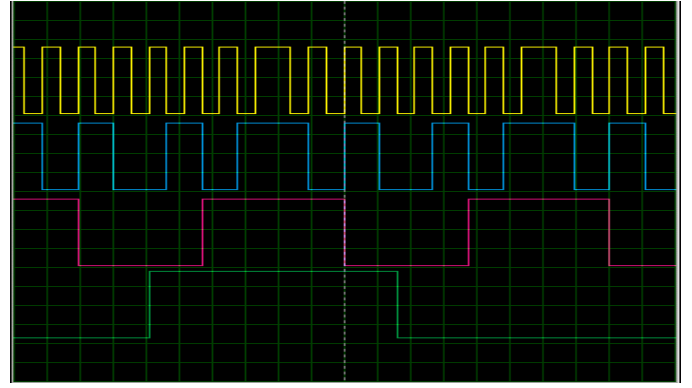


Fig. 30. Asymmetric 15level CHBMLI Output PWM signals for S_1, S_2, S_3 & S_4

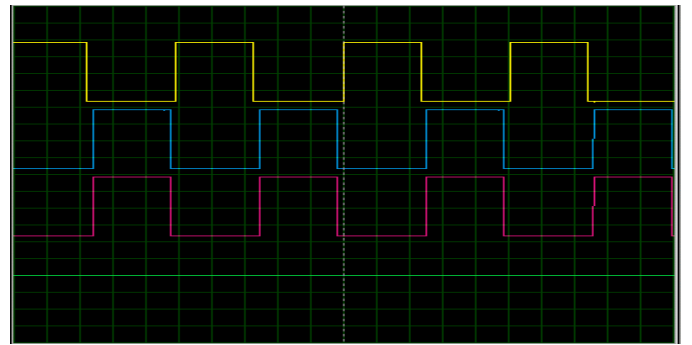


Fig. 31. Asymmetric 15level CHBMLI Output PWM signals for S_5, S_6 & S_7

The 15level ASCHBMLI is designed in Proteus Software as shown in figure 32. In this system a PIC6F877A microcontroller is used to generate the low and high switching frequency for Inverter. A MOSFET driver IC IR2112 is used for Boosting the Gate pulse from the microcontroller. The ASCHBMLI consists of 3 DC voltage source of $8V_{DC}$, $16V_{DC}$ and $32V_{DC}$. An IRF640 Mosfet is connected in series with DC source and Diode is connected in parallel with the Mosfet and DC source. Figure 29 shows the Gate pulse for Switch S_1, S_2, S_3 and S_4 . Figure 30 shows the Gate Pulse of Cascaded H-Bridge inverter of switch S_5, S_6 and S_7 .

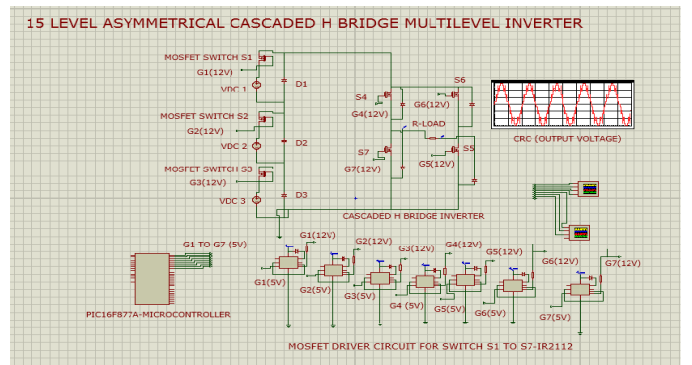


Fig. 32. A 15 Level ASCHB MLI using PROTEUS software

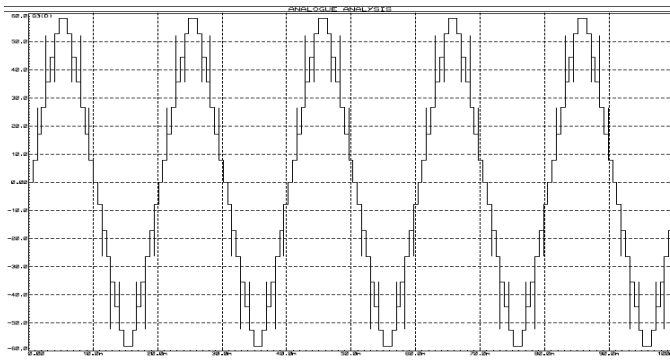


Fig. 33. Asymmetric 15level CHBMLI Output voltage

Figure 33 shows the Asymmetrical Cascaded H Bridge Multilevel inverter for output voltage waveform. The input DC voltage source are $8V_{dc}$, $16V_{dc}$, & $32V_{dc}$. The output voltage levels are $8V_{dc}$, $16V_{dc}$, $24V_{dc}$, $32V_{dc}$, $40V_{dc}$, $48V_{dc}$, $56V_{dc}$, $0V_{dc}$, $-8V_{dc}$, $-16V_{dc}$, $-24V_{dc}$, $-32V_{dc}$, $-40V_{dc}$, $-48V_{dc}$, $-54V_{dc}$ respectively. [10]

VI. SEXPERIMENTAL RESULT ANALYSIS



Fig. 34. 15-Level Asymmetrical CHBMLI with RL Load by using PIC16F877A

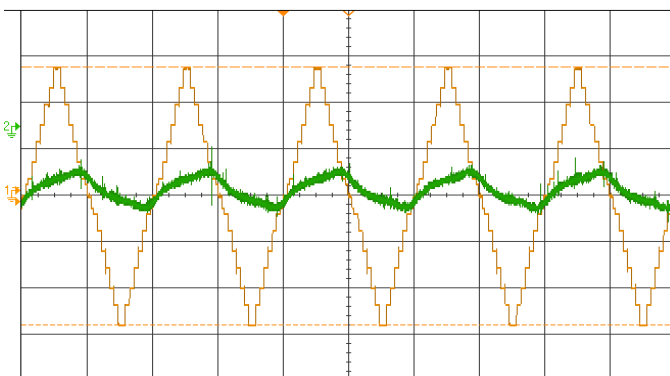


Fig. 35. Output voltage and current waveform for 15-level ASCHBMLI using RL Load

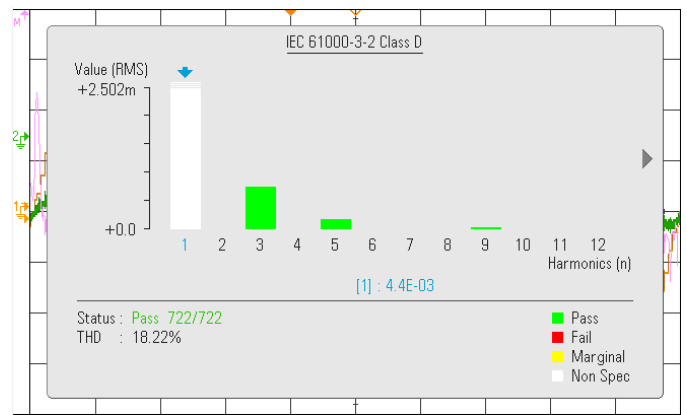


Fig. 36. THD analysis for ASCHBMLI using RL Load

In Figure 34 shows the ASCHBMLI using RL load using PIC16F877A Microcontroller for a real time system. The input DC voltage are $4V_{dc}$, $8V_{dc}$ and $16V_{dc}$ respectively. The Output voltage levels are $28V_{dc}$, $24V_{dc}$, $20V_{dc}$, $16V_{dc}$, $12V_{dc}$, $8V_{dc}$, $4V_{dc}$, $0V_{dc}$, $-4V_{dc}$, $-8V_{dc}$, $-12V_{dc}$, $-16V_{dc}$, $-20V_{dc}$, $-24V_{dc}$, $-28V_{dc}$. The output voltage levels and current waveform are shown in figure 35. In Figure 34 shows the THD analysis for ASCHBMLI using RL Load.

VII. CONCLUSION

A symmetrical Cascaded H bridge Multilevel inverter (SCHBMLI) and Asymmetrical Cascaded H bridge Multilevel Inverter (ASCHBMLI) using PD-PWM technique have been analysed in this paper. Both Inverters consist of same power semiconductor switches but output voltage levels are different. In SCHBMLI the output voltage is 9 level, whereas ASCHBMLI the output voltage level is 15 level. The THD analysis for ASCHBMLI is 7.21%, whereas THD analysis for SCHBMLI is 22.00%. In this system the THD is very less in ASCHBMLI and it is implemented in real time system using PIC16F877A microcontroller with RL load. This type of proposed system is used for high power applications in photovoltaic and its reduce overall cost as well as size of the system.

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