COMPARATIVE ANALYSIS OF TRAPEZOIDAL PWM STRATEGIES FOR THREE PHASE TRINARY SOURCE NINE LEVEL INVERTER

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Abstract: *This paper presents a comprehensive analysis of various bipolar Multicarrier Pulse Width Modulation (MCPWM) strategies with Trapezoidal reference for three phase Trinary Source Nine level cascaded inverter. A new approach of nine levels is for medium voltage applications. The proposed topology uses reduced number of switching devices and thus reducing losses and low THD in comparison with the conventional topology. The configuration of the circuit is simple and easy to control. Performance factors such as %THD, V_{RMS} where measured and Crest Factor (CF), Distortion Factor (DF), Form Factor (FF) of output voltage were calculated for different modulation indices and the results are compared. PDPWM strategy provides minimum THD and COPWM strategy provides higher fundamental V_{RMS} output voltage.*

Key words: *Cascaded Multi Level Inverter (CMLI), Total Harmonic Distortion (THD), Multicarrier Pulse width modulation (MCPWM), Bipolar, minimum switches*

1. Introduction

Multilevel inverter is used to synthesize a nearby sinusoidal voltage from various levels of DC voltages and the proposed cascaded H-bridge inverter is used to reduce the number of switches. The proposed nine level cascaded H-bridge multilevel inverters require a less number of components to obtain the same number of voltage levels when compared to diode clamped and flying capacitor type topologies. The structure requires lesser active switches as compared with conventional cascaded H-bridge topologies. Also, it generally regularises the stair-case voltage waveform from several DC sources which has reduced harmonic content. Mokhberdoran et al [1] designed and implemented a new cascaded symmetric and asymmetric multilevel inverter. Espinosa et al [2] proposed a new modulation method to minimize THD for a 13-level asymmetric inverter. Babaei et al [3] presented a cascaded multilevel inverter with series connection of novel H-Bridge basic units. Najafi et al [4] presented the design and implementation of a new multilevel inverter topology. Bodo et al investigated the carrier-based PWM techniques for a five-phase open-end winding drive topology in [5]. A meticulous analysis of induction motor drive fed from a nine-level cascaded H-Bridge inverter with level shifted multicarrier PWM were discussed in [6]. Chellammall et al investigated the performance of three phase cascaded H-bridge multilevel inverter for under voltage and over voltage conditions in [7]. Balamurugan et al employed multilevel inverter topologies using Flipflops and proposed control techniques for various bipolar PWM strategies of three phase five level cascaded inverter and introduced advanced references and carriers based PWM in a symmetrical inverter in [8,11,12]. Investigations of symmetrical and asymmetrical cascaded H-bridge inverter were carried out in [9]. The PWM control for hybrid clamped multilevel inverters is achieved in [10]. Ilhami Colak reveals the comparison of multicarrier techniques in seven level cascade multilevel inverter and presented the review of multilevel voltage source inverter topologies and its control schemes in [13,16]. Jamuna et al compared MSPWM and MTPWM techniques for asymmetric H-bridge multilevel inverter in [14]. FPGA based single-phase cascaded multilevel voltage source inverter fed ASD applications were developed in [15]. This paper aims at comprehensively analysing the proposed three phase Trinary source nine level cascaded H-bridge inverter using various bipolar Trapezoidal PWM Strategies. In this paper, the aforesaid topology was developed using MATLAB-SIMULINK.

2. Three Phase Nine Level Trinary Source Cascaded Multilevel Inverter

The fundamental H-bridge cascaded topology increases the number of components required, which in

turn makes the design complexity and increases the cost. It is also to be establishing that the maximum output voltage cannot go beyond the sum of voltage of individual sources which becomes the most important setback of this topology. Because of the foresaid reason in an application which requires high output voltage from low voltage level, it needs H-bridge module in addition or step-up transformers. To accomplish this problem a new topology proposed is shown in Fig.1 to reduce the component count.

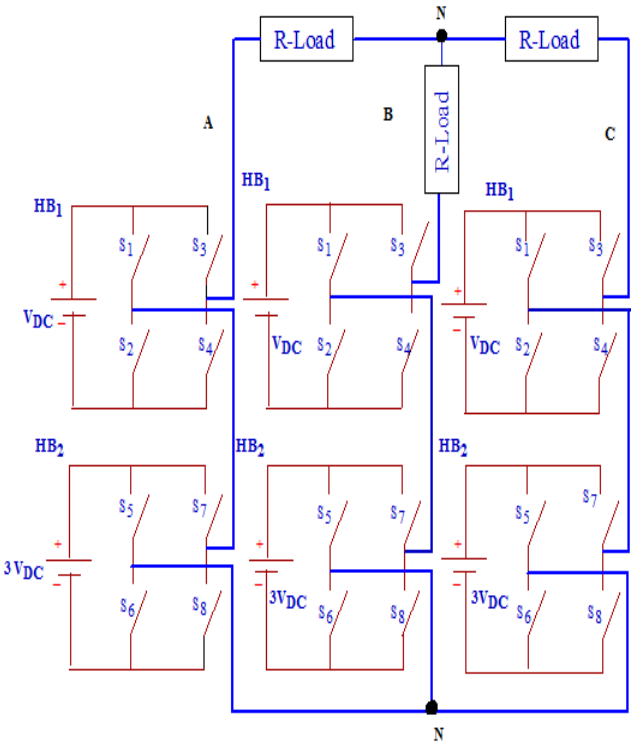

Fig.1. Three phase nine level Trinary source Cascaded inverter

Fig.1 shows the topology of the proposed three phase nine level cascaded Trinary DC source multilevel inverter. It views like a conventional cascaded H-bridge multilevel inverter apart from input DC sources. The topology comprises of floating input DC sources connected through power switches. The structure requires lesser active switches as compared with conventional cascaded H-bridge topology with much reduced switching losses. By using V_{DC} and $3V_{DC}$, it can synthesize nine output levels; $-4V_{DC}$, $-3V_{DC}$, $-2V_{DC}$, $-V_{DC}$, 0, V_{DC} , $2V_{DC}$, $3V_{DC}$ and $4V_{DC}$. The lower inverter generates an elementary output voltage with three levels and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. At this point, the final output voltage level becomes the sum of each terminal voltage of H-bridge [1] and it is given as

$$V_{out} = V_{HB1} + V_{HB2} \quad (1)$$

In the proposed circuit design, suppose the n number of H-bridge component has self-governing DC sources in sequence of the power of 3, a predictable output voltage level is given as

$$V_n = 3^n,\ n = 1,2,3,..... \quad (2)$$

where; n is number of H bridges.

Waveforms of output voltage are denoted as (V_{out}), upper terminal voltage is (V_{HB1}) and the lower voltage is (V_{HB2}) inverter in sequence. The output voltage has nine levels include zero level. Though it is close to a sinusoidal wave, it has lower order harmonics. So it needs more H-bridge modules or output filter to obtain high quality output voltages. Advantage of the proposed multilevel inverter scheme is the elimination of transformer in the main power stage. However, each cell of the proposed multilevel inverter requires its own isolated power supply. The provision of these isolated supplies is the main limitation in the power electronic circuit design. So the proposed multilevel inverter is suitable for photovoltaic power generating systems equipped with distributed power sources [7].

3. Multicarrier Trapezoidal Pulse Width Modulation Strategies

The most popular method of controlling the output voltage is by incorporating PWM control within the inverters. In this paper five different modulation strategies were tried in order to increase the output voltage and also to reduce the THD. It is generally recognized that, increasing the switching frequency of the PWM pattern results in reducing lower frequency harmonics. This paper includes reference waveform as trapezoidal and 8 triangular carriers. To synthesize multilevel output AC voltage using different levels of DC inputs, semiconductor devices must be switched ON and OFF in such a way that desired fundamental is obtained with minimum harmonic distortion. There are different types of approaches for the selection of switching techniques for the Trinary source inverters. Among all the PWM methods for Trinary source cascaded inverter, carrier based PWM methods and space vector methods are often used but when the number of output levels is more than five, the space vector method will be very complicated with the increase of switching states. So the carrier based PWM strategy is preferred under this condition in Trinary

source inverters. This paper focuses on carrier based PWM strategies which have been extended for use in Trinary inverter by using multiple carriers. Multicarrier based PWM strategies have more than one carrier that can be triangular waves or sawtooth waves and so on. The carrier waves can be either bipolar or unipolar. In this paper, a comprehensive analysis of the afore mentioned topology is carried out using bipolar MCPWM strategies. In this paper, various MCPWM strategies like Phase Disposition (PD), Phase Opposition Disposition (POD), Alternative Phase Opposition Disposition (APOD), Variable Frequency (VF) and Carrier Overlapping (CO) were proposed for three phase nine level Trinary source cascaded inverter. For an m-level inverter using bipolar multicarrier strategy, (m-1) carriers with same frequency f_c and same peak-to-peak amplitude A_C are used. The reference waveform has amplitude A_m and frequency f_m are placed at zero reference. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched ON. Otherwise, the device switched OFF. In this paper, the frequency ratio m_f =40 and modulation index m_a is varied from 0.8 to 1.

$$m_f = f_c/f_m \quad (3) \text{ except for VFPWM}$$

$$m_a = 2A_m/(m\text{-}1)A_c \quad (4) \text{ except for COPWM}$$

3.1. Phase Disposition (PD) PWM Strategy

The Principle of PDPWM strategy is to use the several carriers with single modulating waveform. In Phase Disposition all the carriers are in phase and the carriers are disposed so that the bands they occupy are contiguous. The modulation wave is centered in the middle of the carrier set. Fig.2 shows the multicarrier arrangement for PDPWM strategy for m_a = 0.9 and m_f = 40.

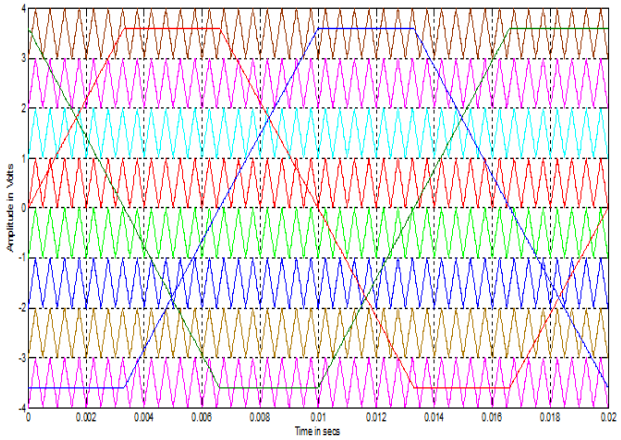

Fig.2. Carrier arrangement for PDPWM Strategy

3.2. Phase Opposition Disposition (POD) PWM Strategy

With the PODPWM method the carrier waveforms above the zero reference value are in phase. The carrier waveforms below zero are also in phase but are 180° phase shifted from those above zero. Fig.3 shows the multicarrier arrangement for PODPWM method for m_a = 0.9 and m_f = 40.

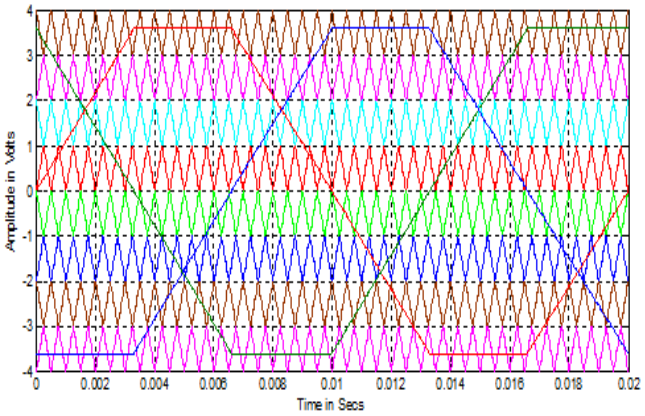

Fig.3. Carrier arrangement for PODPWM Strategy

3.3. Alternative Phase Opposition Disposition (APOD) PWM Strategy

This method requires each of the eight carrier waves for a nine level inverter to be phase displaced from each other by 180° alternately. Fig.4 shows the multicarrier arrangement for APODPWM method for m_a = 0.9 and m_f = 40.

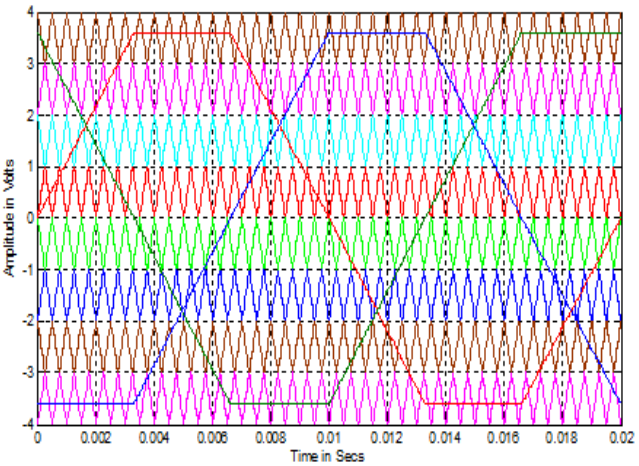

Fig.4.Carrier arrangement for APODPWM Strategy

3.4. Variable Frequency (VF) PWM Strategy

The number of switchings for upper and lower devices of chosen nine level three phaseTrinary cascaded DC source inverter is much more than that of intermediate switches in constant frequency carriers. In order to equalize the number of switchings for all the switches, variable frequency PWM strategy is used as illustrated

in Fig.5, in which the carrier frequency of the intermediate switches is properly increased to balance the number of switchings for all the switches.

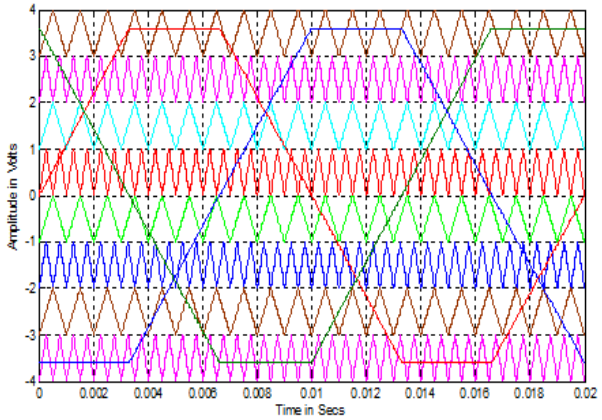

Fig.5.Carrier arrangement for VFPWM Strategy

3.5.Carrier Overlapping (CO) PWM Strategy

In the Carrier Overlapping strategy, m-1 carriers are disposed such that the bands they occupy overlap each other, the overlapping vertical distance between each carrier is A_C /2 (A_C =1). The reference waveform is centred in the middle of the carrier signals. The amplitude modulation index m_a is defined as follows:

$$m_a = A_m/(2.5 \times A_c) \quad (5)$$

The vertical offset of carriers for nine-level inverter with COPWM strategy is shown in Fig.6.

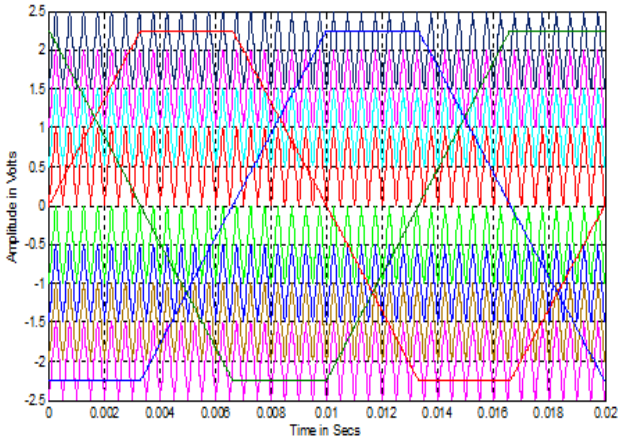

Fig.6.Carrier arrangement for COPWM Strategy

4. Simulation Results

The nine level three phase Trinary cascaded DC source inverter is modeled in SIMULINK using Power System block set. Switching signals for Trinary cascaded DC source inverter are developed using multicarrier trapezoidal PWM strategies. Simulations are performed for different values of m_a ranging from 0.8 –1.

Figs.7–17 show the simulated output voltage of three phase Trinary cascaded DC source inverter with their corresponding FFT plots shown for only one sample value of m_a = 0.9 for above said PWM strategies. Fig.17 shows a graphical comparison of %THD for various strategies for different modulation indices.

The corresponding %THD (a measure of closeness in shape between a waveform and its fundamental component) is measured using the FFT block and their values are listed in Table 1. Table 2 shows the Distortion Factor of the output voltage of chosen MLI. Table 3 displays the V_{RMS} of fundamental inverter output (a measure of DC bus utilization). Table 4 display the corresponding Crest Factor (used to specify peak current rating of the devices). Table 5 display the consequent Form Factor (related to power quality issues).The following parameter values are used for simulation: V_{DC} =100V, $3V_{DC}$ =300V, f_m = 50Hz, f_c=2000Hz and load (R=100Ω).

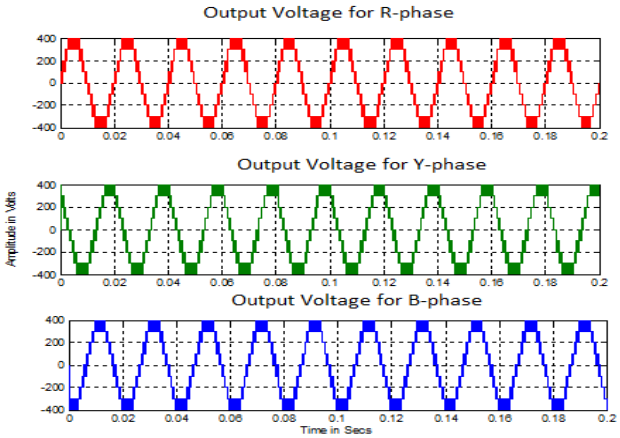

Fig.7.Output Voltage generated by PDPWM Strategy

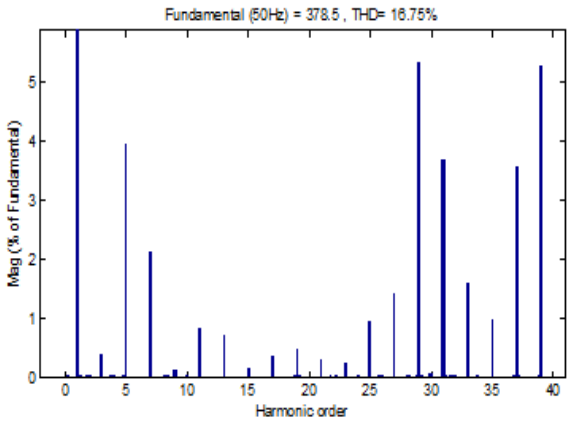

Fig.8.FFT Plot for Output Voltage of PDPWM Strategy

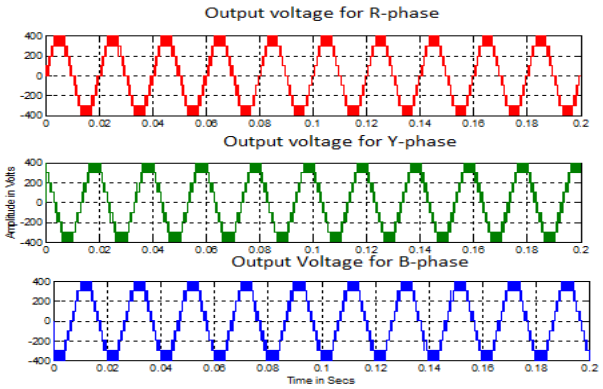

Fig.9.Output Voltage generated by PODPWM Strategy

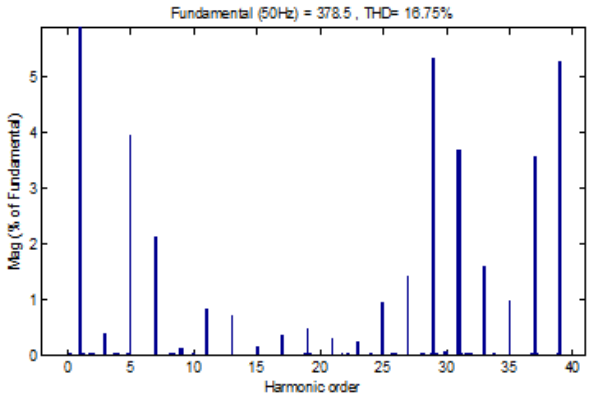

Fig.10.FFT Plot for Output Voltage of PODPWM Strategy

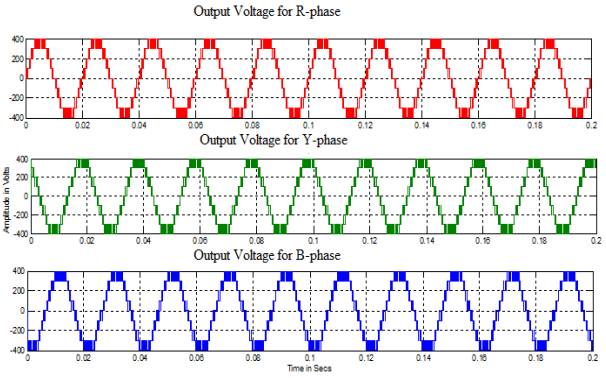

Fig.11.Output Voltage generated by APODPWM Strategy

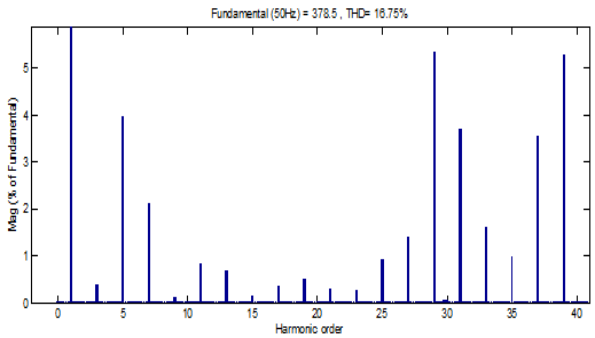

Fig.12.FFT Plot for Output Voltage of APODPWM Strategy

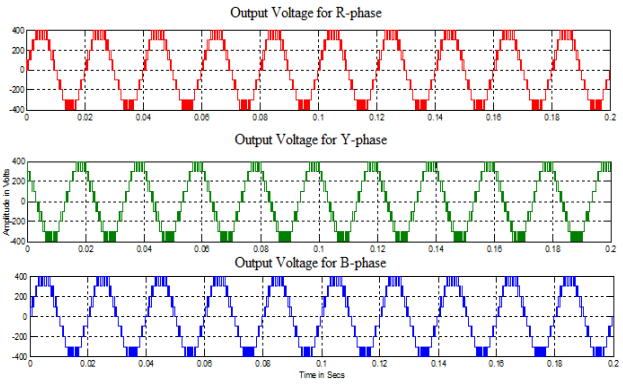

Fig.13.Output Voltage generated by VFPWM Strategy

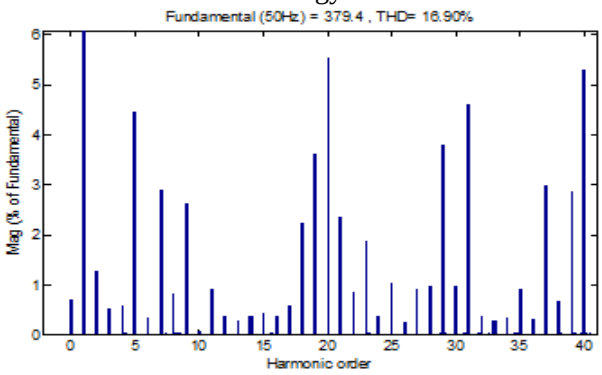

Fig.14.FFT Plot for Output Voltage of VFPWM Strategy

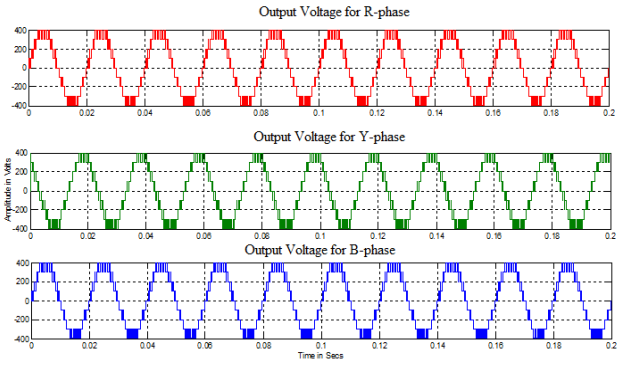

Fig.15.Output Voltage generated by COPWM Strategy

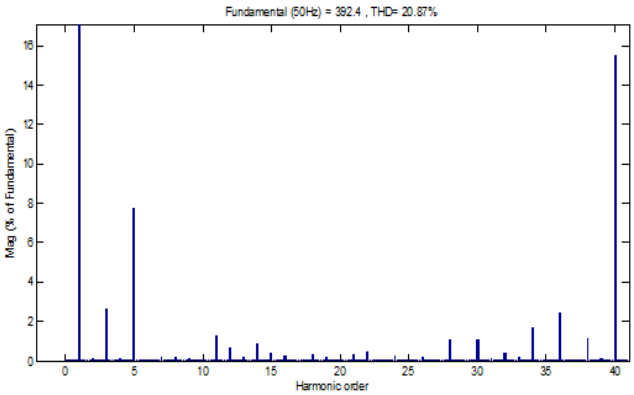

Fig.16.FFT Plot for Output Voltage of COPWM Strategy

Table 1
%THD for Different Modulation Indices

m_a	PD	POD	APOD	VF	CO
1	12.08	12.17	12.17	12.40	16.97
0.95	15.12	15.15	15.23	15.44	19.17
0.9	17.00	16.75	16.75	16.90	20.87
0.85	17.60	17.72	17.72	16.71	22.69
0.8	17.41	17.39	17.39	16.99	24.17

Table 2
% Distortion Factor for Different Modulation Indices

m_a	PD	POD	APOD	VF	CO
1	0.1711	0.1665	0.1665	0.2227	0.2996
0.95	0.1745	0.1674	0.1693	0.2974	0.3418
0.9	0.1993	0.1702	0.1702	0.3767	0.4228
0.85	0.2059	0.1724	0.1724	0.4012	0.5383
0.8	0.2234	0.1756	0.1756	0.4306	0.4228

Table 3
% V_{RMS} (Fundamental) for Different Modulation Indices

m_a	PD	POD	APOD	VF	CO
1	297.2	297.1	297.1	297.7	300.6
0.95	282.3	282.3	282.4	283.3	289.2
0.9	267.6	267.6	267.6	268.3	277.5
0.85	252.7	252.8	252.8	252.7	265.3
0.8	237.8	237.9	237.9	237.5	252.7

Table 4
% Crest Factor for Different Modulation Indices

m_a	PD	POD	APOD	VF	CO
1	1.414	1.414	1.414	1.414	1.414
0.95	1.414	1.414	1.413	1.414	1.414
0.9	1.414	1.414	1.414	1.414	1.414
0.85	1.413	1.414	1.414	1.414	1.414
0.8	1.414	1.414	1.414	1.414	1.414

Table 5
Form Factor for Different Modulation Indices

m_a	PD	POD	APOD	VF	CO
1	3.715E+3	0.0297E+6	0.0297E+6	1.6538E+3	6.012E+3
0.95	4.0328E+3	INF	0.0282E+6	2.5754E+3	9.64E+3
0.9	8.92E+3	0.0267E+6	0.0267E+6	0.3832E+3	5.55E+3
0.85	0.4859E+3	0.0126E+ 6	0.0126E+6	0.1419E+3	4.4216E+3
0.8	0.8774E+3	INF	INF	0.1870E+3	3.61E+3

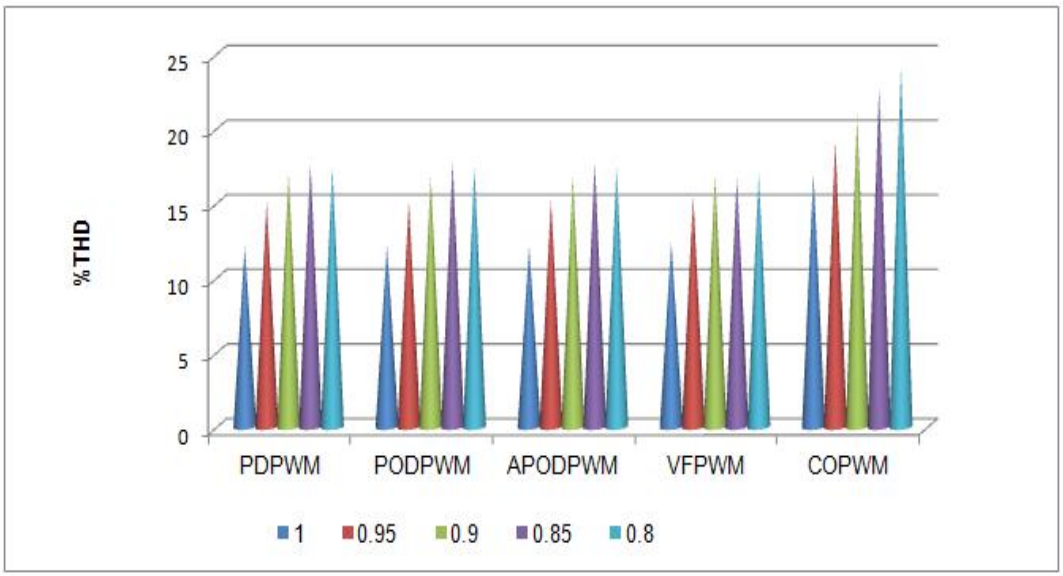

Fig.17. % THD V_S m_a

It is observed from Table 1 that the harmonic content is found to be minimum in PDPWM and maximum in COPWM strategy for chosen modulation indices. Table 2 shows that the variation in harmonic content of the output voltage after second order attenuation indicated by %DF is relatively less in both PODPWM and APODPWM strategies . From Table 3, it is found that the COPWM strategy provide relatively higher DC bus utilization. It is inferred from Table 4 that Crest Factor is almost same for all the techniques of the simulated output voltage. Table 5 indicates that PODPWM and APODPWM strategies have higher Form Factor.

5. Conclusion

In this paper, various multicarrier PWM strategies for chosen nine level three phase Trinary cascaded DC source inverter have been developed and simulation results are presented for different modulation indices ranging from 0.8-1.Various performance factors like %THD, DF, V_{RMS} of fundamental, CF and FF have been evaluated, presented and analysed. It is observed that PDPWM strategy provides lower THD. PODPWM and APODPWM strategies provide relatively lower DF. The maximum DC bus utilization is achieved in COPWM strategy (Table 3). CF is almost same for all the strategies (Table 4). Higher FF is obtained in PODPWM and APODPWM Strategies (Table 5). The result indicates that appropriate PWM strategies may be employed depending on the performance measure required in a particular application of Trinary DC source inverter.

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