ASYMMETRICAL MULTILEVEL INVERTER TOPOLOGIES TO REDUCE THE SEMICONDUCTOR SWITCHES AND DC SOURCES

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Abstract: *In this paper two novel topologies of asymmetrical multilevel inverter have been presented. Each topology is based on the concept of additive and subtractive combination of different DC sources. The proposed topologies have same structure when two DC sources are used; but, for more than two DC sources, each topology has different structure, number of semiconductor devices and number of output voltage levels. Figure of merit (FOM) for multilevel inverter is defined in this paper and calculated for various topologies including the proposed topologies. For proposed topologies, new multi carrier sinusoidal pulse width modulation (MC-SPWM) has been adopted to generate the output voltage levels of an inverter. High number of levels have been obtained by using less number of DC sources and unidirectional semiconductor devices in comparison to existing topologies. In this paper, simulation is done in MATLAB/ SIMULINK environment. The output voltage, load current and total harmonic distortion (THD) has been calculated.*

Key words: *Asymmetrical multilevel inverter, Multi carrier sinusoidal pulse width modulation, Figure of merit, Total harmonic distortion*

1. Introduction

Due to environmental problems and lack of fossil fuels, use of renewable energy is increasing day by day. The power electronic converter`s cost, power quality, efficiency space and reliability are the main key factor to integrate converter with renewable energy like solar energy, wind energy etc [1 and 2]. To increase the power quality, first three level multilevel inverter (MLI) has been reported initially in [3]. With the significant changes in the converter topology, MLI can be categorized into three categories 1) symmetrical MLI, 2) asymmetrical MLI 3) S-DCMI [4, 5 and 6]. The first two types of topologies use more than one DC source and more number of switching devices viz. MOSFET, IGBT etc to increase the number of levels in output voltage [7].

The 15 level multilevel inverter using series and parallel DC sources is used to increase the number of levels by using H bridge and 11 semiconductor switches [7]. A new concept of additive or subtractive combination of different DC sources based multilevel inverter has six unidirectional semiconductor switches and two bidirectional semiconductor switches to generate twenty seven output voltage levels using 3 DC sources [8]. The demerit of this multilevel inverter is that it constitutes bi-directional semiconductor switches, which further enhance the number of switches, switching and conduction losses in comparison to the unidirectional device. Additionally, a 5-level multilevel inverter using addition or subtraction principle of different DC sources is compared with conventional 5-level inverter [9].

A symmetrical inverter has been implemented comprising three main parts of an inverter as DC sources, main switches and one H-bridge cell using bidirectional switches [10]. The main objective of this inverter has been to reduce the number of switches, losses, installation area and cost with application as Dynamic Voltage Restorer (DVR) for improving power quality. Asymmetric and symmetric topologies are suggested to reduce the number of switching devices for specified number of output voltage levels [11, 12]. Three algorithms to select magnitude of different DC sources has been reported and implemented on optimal structure MLI [12]. Cascaded cross-switched MLI topology is used as symmetric and asymmetric MLI [13]. To reduce the switching losses, THD and to increase the efficiency a 47 level switch-ladder MLI topology has been reported [14]. This topology is used a multiwinding transformer to create higher number of levels with H-bridge. To reduce the DC sources, cascade hybrid multilevel topology of asymmetric MLI has been reported which uses one H-bridge for each phase with a bottom three leg inverter [15]. An optimal structure has been used to reduce the switches, DC sources, standing voltage and to maximize the number of levels [15].

In this paper, two asymmetric topologies of MLIs have been proposed. In section 2, new structure of two topologies has been given. In section 3, a scheme to select magnitude of different DC sources for the proposed topologies has been presented. In section 4, details of the proposed modulation scheme has been explained. In section 5 the proposed topologies have been compared with existing topologies. Section 6 includes simulation results of output voltage and output current of twenty one

levels using first topology (P1) and twenty seven levels using second topology (P2). Section 7 concludes the paper.

2. Structure of The Proposed Topologies

The proposed topologies structure depends upon the number of DC sources used. As the DC sources increases, both topologies change its structure to make a higher number of combinations of DC sources. The structure of the proposed topology and combination of different DC sources is as under:

A. First Proposed Topology (P1)

The first proposed topology of asymmetrical MLI is shown in Fig. 1. All the DC sources $E_1 - E_N$ have different magnitude to obtain higher number of levels. If N numbers of DC sources are used, then numbers of unidirectional semiconductor switches constituting the topology are as under:

$$4N \text{ if } N < 3 \quad (1)$$

$$4N - 2 \text{ if } N = 3 \quad (2)$$

$$4N - 4 \text{ if } N > 3 \quad (3)$$

In P1, for only three DC sources, structure is different from that shown in Fig. 1 i.e. switches S_7, S_8 and DC source E_{22} are not included; but, for more than three DC sources, structure will be same as given in Fig. 1. The number of semiconductor devices when N number of DC sources is used is given in Table I as per the topology of Fig. 1. When one DC source is used, then the maximum number of levels will be three as E_1, 0, $-E_1$, When two DC sources are used, then the number of levels will be nine as explained in latter section. For three DC sources, maximum number of levels will be twenty one as given in Table II. When four DC sources are used, the number of levels will be one hundred forty one. As the number of DC sources increases, number of combination of DC sources increases and hence the output voltage levels increases. In this paper, numbers of levels are calculated up to four DC sources only.

For three DC source, switching states and combination of DC sources for the P1 is shown in Table II. It can be observed that to create a level, five switches will be ON and the others switches will be in OFF condition.

By changing the switching arrangement of semiconductor switches, different output voltage levels can be obtained. There are some pair of switches in the proposed topology that should not operate simultaneously; otherwise, short circuit can take place. According to the proposed structure when n number of switches are used then S_1, S_2; S_3, S_4; S_5, S_6; ..... S_{n-3}, S_{n-2}; and S_{n-1}, S_n switches pair should not operate together.

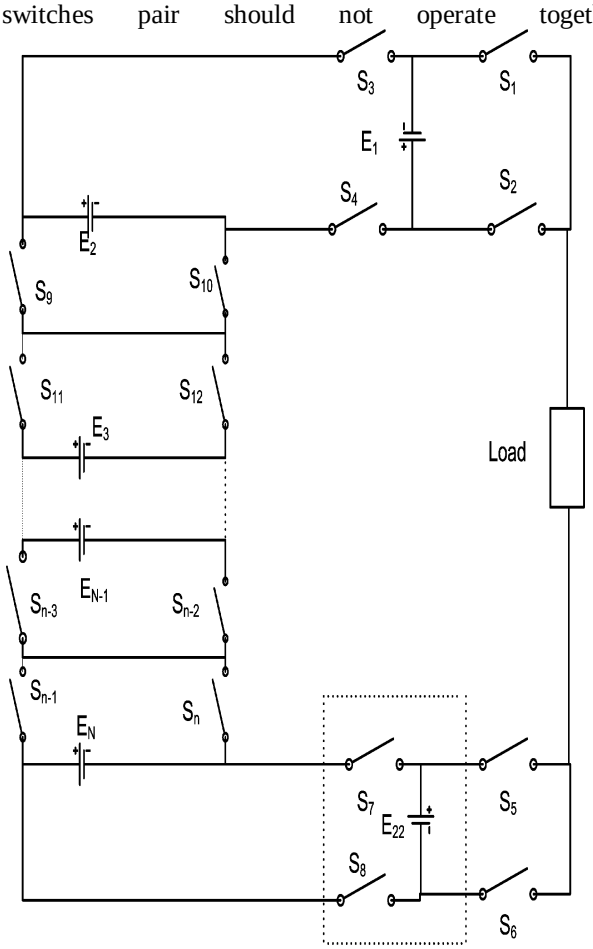

Fig. 1. Structure of first proposed topology

TABLE I

Semiconductor switches participating in conduction for different number of DC sources

Number of DC sources, (N)	Switches and battery sources used
1	S_1, S_2, S_3, S_4, E_1
2	S_1, S_2, S_5, S_6, S_9, S_{10}, S_{11}, S_{12}, E_2, E_3
3	S_1, S_2, S_5, S_6, S_7, S_8, S_9, S_{10}, S_{11}, S_{12} , E_1, E_2, E_3
4	S_1, S_2,S_3, S_4, S_5, S_6, S_7, S_8, S_9, S_{10}, S_{11}, S_{12}, E_1, E_2, E_3, E_{22}

B. Second Proposed Topology (P2)

The second proposed topology is shown in Fig. 2. This topology has advantage that it produces high number of levels using less DC sources in comparison to the P1.

TABLE II
Switching states of twenty one level using first proposed topology

Pulse Mode	DC sources combination	Switches states, 1 = ON, 0 = OFF									
		S_1	S_2	S_3	S_4	S_5	S_6	S_9	S_{10}	S_{11}	S_{12}
G_1	E_3	1	0	1	0	1	0	1	0	1	0
G_2	E_2-E_3	1	0	1	0	0	1	0	1	0	1
G_3	E_2	1	0	1	0	1	0	0	1	0	1
G_4	E_1-E_3	0	1	1	0	0	1	1	0	0	1
G_5	E_2+E_3	1	0	1	0	1	0	0	1	1	0
G_6	E_1	0	1	1	0	0	1	1	0	1	0
G_7	E_1+E_3	0	1	1	0	1	0	1	0	1	0
G_8	E_1+E_2-E_3	0	1	1	0	0	1	0	1	0	1
G_9	E_1+E_2	0	1	1	0	1	0	0	1	0	1
G_{10}	E_1+E_2+E_3	0	1	1	0	1	0	0	1	1	0
-G_1	-E_1-E_2-E_3	1	0	0	1	0	1	1	0	0	1
-G_2	-E_1-E_2	1	0	0	1	0	1	1	0	1	0
-G_3	-E_1-E_2+E_3	1	0	0	1	1	0	1	0	1	0
-G_4	-E_1-E_3	1	0	0	1	0	1	0	1	0	1
-G_5	-E_1	1	0	0	1	0	1	0	1	0	1
-G_6	-E_2-E_3	0	1	0	1	0	1	1	0	0	1
-G_7	-E_1+E_3	1	0	0	1	1	0	0	1	1	0
-G_8	-E_2	0	1	0	1	0	1	1	0	1	0
-G_9	-E_2+E_3	0	1	0	1	1	0	1	0	1	0
-G_{10}	-E_3	0	1	0	1	0	1	0	1	0	1

In [8], an asymmetrical multilevel structure has been reported which uses same principle to obtain same number of levels as used in this proposed topology; but, difference is that the proposed topology uses less semiconductor devices; because, it needs just unidirectional devices. The basic principle of this topology is same as described in [8].

If N numbers of DC sources are used, then numbers of unidirectional semiconductor devices required are $4N$. In this topology also some pair of switches should not operate simultaneously; otherwise, short circuit occurs. According to the proposed structure when n number of switches are used then S_1, S_2; S_3, S_4; S_5, S_6; ..... S_{n-3}, S_{n-2}; and S_{n-1}, S_n switches pair should not operate simultaneously.

3. DC Sources Arrangement

Various DC source arrangements have been reported for different MLI topologies [16, 17]. These proposed topologies have different algorithm to select the magnitude of different DC sources.

Arrangement for two and three DC sources for the proposed MLI topologies is as under:

1. Using two DC sources

$$E_1 = \alpha_1 V_d \quad (4)$$

$$E_2 = \alpha_2 V_d \quad (5)$$

Total DC voltage, $V_d = E_1 + E_2$ (6)

$\alpha_1 = 0.62$, $\alpha_2 = 0.377$ (7)

1. Using three DC sources

Total DC voltage, $V_d = E_1 + E_2 + E_3$ (8)

$$E_1 = \alpha_1 V_d \quad (9)$$

$$E_2 = \alpha_2 V_d \quad (10)$$

$$E_3 = \alpha_3 V_d \quad (11)$$

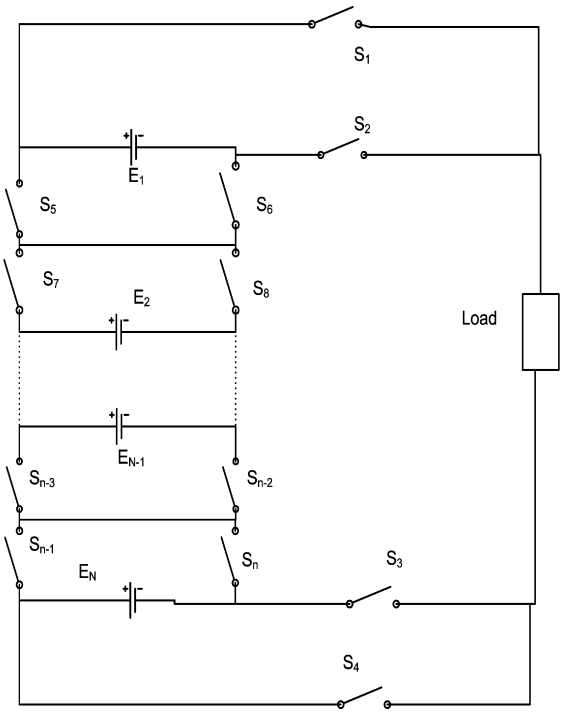

Fig. 1. Structure of second proposed topology

Here E_1, E_2, E_3 is magnitude of different DC sources.

The value of α_1, α_2, α_3 are selected as 0.534, 0.347 and 0.117. To reduce THD of the output voltage, the value of alphas can be optimized; but, it is not the objective of this paper

4. Modulation Scheme for The Proposed Topologies

Selective Harmonic Elimination (SHE) PWM technique is used for eleven level cascade MLI. Furthermore, optimization technique has been reported to optimize the angles of the output voltage to reduce the THD [18, 19]. Several PWM techniques have been reported for MLI [20]. These techniques can be broadly classified as high frequency and fundamental frequency techniques. Under the category of SPWM, THD is calculated for seven level cascaded MLI. It has been reported that phase shifted

pulse width SPWM gives better results than other SPWM techniques [21].

For the proposed topologies, MC-SPWM scheme is used to obtain output voltage levels. The P1 uses MC-SPWM to create twenty one level of output voltage as shown in Fig. 3. The levels in positive half cycle are obtained by comparing constant wave with sinusoidal wave and levels in negative half cycle also obtained by using same principle as in positive half cycle. The proposed MC-SPWM is combination of fundamental frequency and higher frequency for the proposed topologies. Some switches operates at fundamental frequency and some switches operates at higher frequency. For the proposed topologies, the carrier wave has a constant level and reference wave is a sinusoidal wave. To obtain L number of levels in output voltage, $L-1$ carrier waves are required. Fig. 3 shows the carrier and reference waves for twenty one level inverter using the P1.

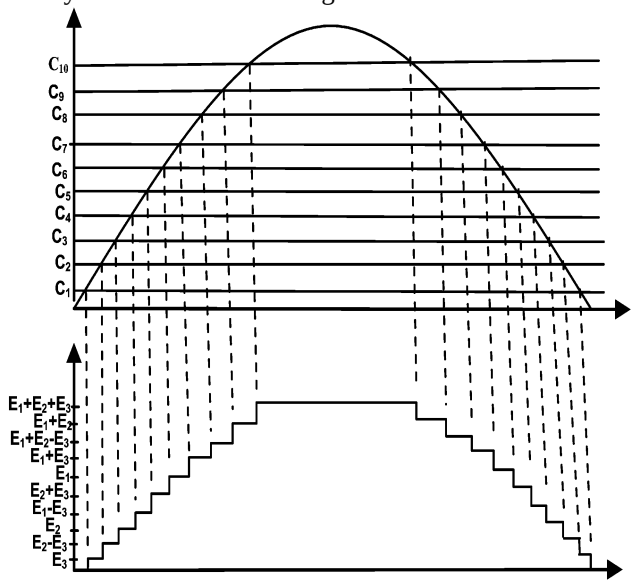

Fig. 3. Multicarrier sinusoidal pulse width modulation for positive half cycle

Pulse modes G_1-G_{10} can be obtained by following Boolean operations:

$$G_1 = C`_1 \oplus C`_2 \quad (12)$$

$$G_2 = C`_2 \oplus C`_3 \quad (13)$$

$$G_3 = C`_3 \oplus C`_4 \quad (14)$$

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$$G_9 = C`_9 \oplus C`_{10} \quad (15)$$

$$G_{10} = C`_{10} \quad (16)$$

Here $\oplus$ stands for Ex-OR operation G_1, $G_2 \ldots . G_{10}$ are the pulse modes and $C_1, C_2, \ldots C_{10}$ are carrier waves as shown in Fig. 3. $C`_1$, $C`_2, \ldots C`_{10}$ is the logical output obtained by comparing carrier waves with sinusoidal wave. Logical output will be high when sinusoidal wave is greater than that of carrier waves.

The lowest and highest magnitude of P1`s output voltage level can be obtained by DC sources combination E_3 and $E_1 + E_2 + E_3$ called G_1 and G_{10} respectively as shown in Fig. 3. By selecting proper pulse mode combinations as given in TABLE II, the desired output of multilevel inverter can be achieved.

5. Comparison of The Proposed Topologies With That of Existing MLIs

To compare the topologies of MLIs, number of component is the main factor. In order to show the capabilities of the proposed inverter topologies, both the topologies are compared with existing topologies. These comparisons have been made on the basis of number of levels, number of DC sources and number of semiconductor devices used. In the proposed topologies only unidirectional semiconductor devices have been used instead of bidirectional devices.

TABLE III
Comparison of the proposed topologies with classic topologies of MLIs

Voltage levels	**Components name**	**Classic multilevel topologies [1, 2, 3, 19]**			**P1**	**P2**
		CMLI	DCMLI	FCMLI		
9	DC sources	4	8	8	2	2
	Freewheeling diode	16	16	16	8	8
	Clamping diode	-	56	-	-	-
	Clamping capacitor	-	-	28	-	-
	Semiconductor devices	16	16	16	8	8
21	DC sources	10	20	20	3	-
	Freewheeling diode	40	40	40	10	
	Clamping diode	-	380	-	-	
	Clamping capacitor	-	-	190	-	
	Semiconductor devices	40	40	40	10	
27	DC sources	13	26	26	-	3
	Freewheeling diode	52	52	52		12
	Clamping diode	-	650	-		-
	Clamping capacitor	-	-	325		-
	Semiconductor devices	52	52	52		12

The topologies have been compared on the basis of number of semiconductor devices versus number of output voltage levels as shown in Fig. 4. It can be seen that P1 uses only twelve semiconductor devices to generate one hundred forty one levels. In comparison to the other topologies, the proposed topology uses less switches to generate the same number of levels.

P2 uses sixteen semiconductor devices to generate one hundred sixty one levels, but; the P2 uses more switches in comparison to the P1; but, it uses fewer switches in comparison to the other existing topologies.

Second comparison has been done on the basis of number of DC sources used and number of output voltage levels obtained as shown in Fig. 5. It can be inferred that the P2 uses equal or less number of DC sources to generate the same number of levels in comparison to the existing topology given in [8]. It generates twenty seven levels using three dc sources and one sixty one levels using only four DC sources. P1 generates twenty one level using three DC sources and one forty one levels using four DC sources, which is less than that of P2; but, it uses less switches.

In Table III, the proposed topology has been compared with classic MLI topologies. It can be observed that both proposed topologies generate higher number of levels using less switches and DC sources than classic multilevel topologies. There is no need of any clamping diode and flying capacitor in the proposed topologies as required in classic topologies.

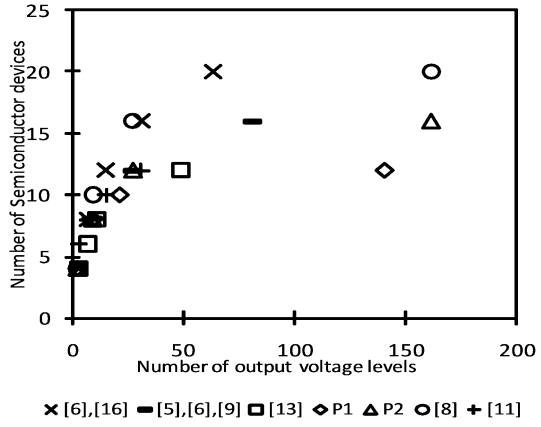


Fig. 4. Comparison between semiconductors devices used to achieve the desired number of output voltage levels

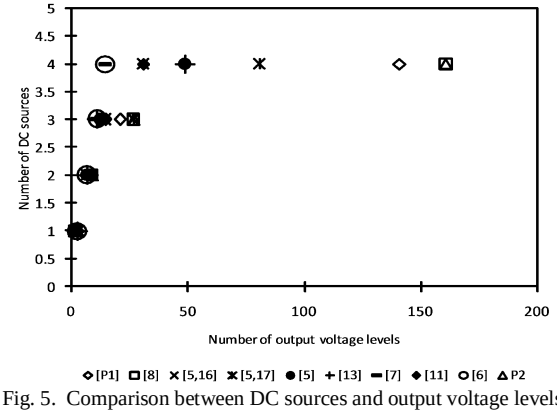


Fig. 5. Comparison between DC sources and output voltage levels

The proposed MLI topologies are compared on the basis of a figure of merit (FOM) defined as under:

$$\text{Figure of merit (FOM)} = \frac{\text{No. of output voltage levels}}{\text{No. of DC sources} \times \text{No. of semiconductor devices}}$$

It can be observed from Table IV that FOM of the proposed topologies is more than that of other topologies. FOM of P1 is higher than that of P2.

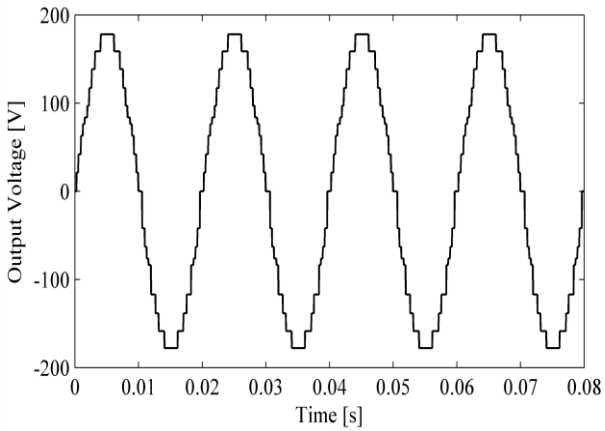
TABLE IV
FOM of various topologies of MLIs

Ref.	Figure of merit (FOM)
[1]	0.14
[6]	0.31
[7]	0.375
[22]	0.39
[16]	0.48
[11]	0.64
[23]	0.77
[5]	1.02
[13]	1.02
[17]	1.26
[8]	1.82
P2	2.51
P1	2.93

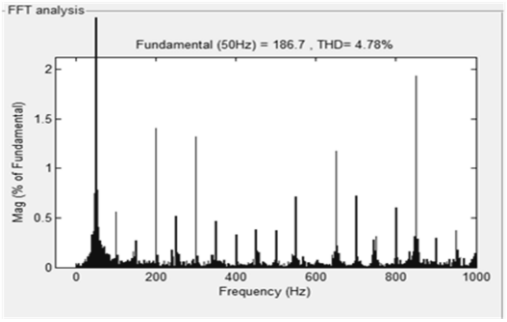
6. Simulation Results

To evaluate the study of proposed topologies, circuit simulation is completed by MATLAB/SIMULINK. The R-L load is connected and performances of both the topologies are studied in detail. The proposed topologies generate 50 Hz frequency. The proposed inverter is programmed using MC-SPWM scheme and results have been obtained by simulation of twenty one level using P1, twenty seven level using P2

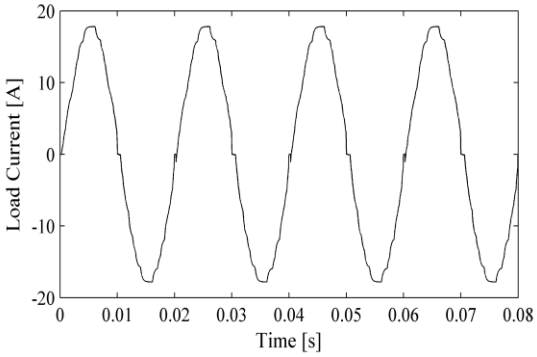
The results have been obtained for P1and P2 by simulation of output voltage and output current. THD has been calculated of output voltage for both the topologies. When three DC sources are used, Fig. 5 and Fig. 6 show the output voltage of MLI, THD of output voltage, Load current using P1 and P2 respectively. The magnitude of E_1 (100V), E_2 (65V) and E_3 (22V) has been selected as described in algorithm.



(a)

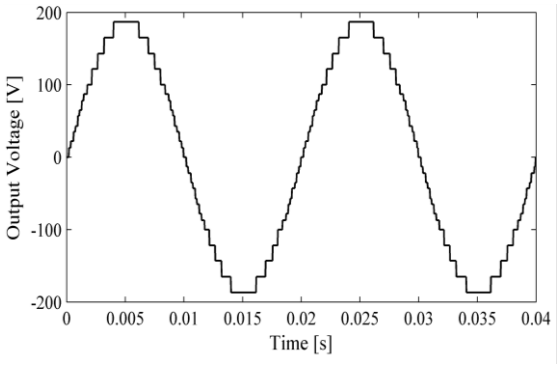


(b)

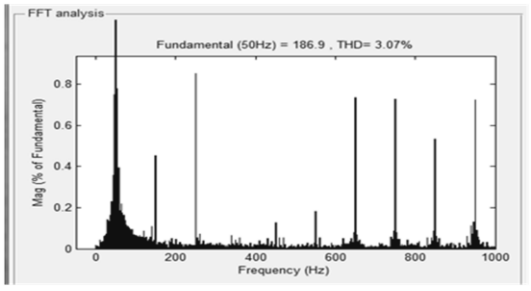


(c)

Fig. 5. Simulation results (a) Output voltage of twenty one level inverter using P1, (b) Harmonic spectrum of output voltage, (c) Load current with RL load (R=10Ω, L=3mH)



(a)



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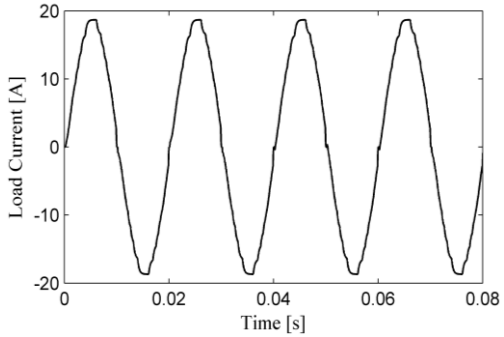

(c)

Fig. 6. Simulation results (a) Output voltage of twenty seven level inverter using P2, (b) Harmonic spectrum of output voltage, (c) Load current with RL load (R=10Ω, L=3mH)

Fig. 5 (a) and Fig 5(b) show the 21-level output voltage and THD of output voltage respectively. The THD is below 5 % of the fundamental voltage. The load current, when R-L load is connected is shown in Fig. 5 (c) for P1

Fig. 6 (a) and Fig. 6 (b) show the 27-level and their THD respectively. The THD is 3.07 %, which is below 5 %. The load current, when R-L load is connected is shown in Fig. 6 (c).

7. Conclusion

Two new topologies using switched DC source principle has been proposed in this paper. The proposed scheme to select the DC source magnitude for the proposed topologies has been presented. It is analyzed that the proposed topologies use less semiconductor devices and DC sources to create same number of levels as that in existing topologies. FOM is defined and calculated for various topologies. It has been found that the proposed MLI topologies P1 and P2 have more FOM than that of existing MLIs topologies. A new MC-SPWM has been proposed for both the topologies, which gives less than 5% THD in output voltage. The simulation results of output voltage, current and their THD is presented for both the proposed topologies.

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