An Improved Single-Inductor Triple-Output Converter with Predictive Control

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Abstract—This paper proposes a new improved topology and control strategy for a single-inductor, triple-output converter with buck, boost and inverted outputs. In this topology, the inverted output is obtained without feeding back power from the load to the source. This minimizes circulating energy and consequent losses. The topology minimizes hardware and requires only three switches. Operation is possible both in discontinuous and continuous conduction modes. The design considerations of this converter are discussed and simulation results confirm the analysis. A predictive-like control of the converter is performed by direct analytical estimation of the duty cycle based on the inductor current in the present cycle. The regulation of the converter against line and load variations is confirmed through simulation results. Hardware validation is done using a Spartan FPGA system and results are presented. The topology and control are generic and can be scaled to more outputs.

Keywords — SIMO, SIBBI, Single-Inductor Multiple-output, Predictive control,Multi-output

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1. INTRODUCTION

Multiple output converters have become popular in a wide variety of applications and particularly in portable devices. Minimum hardware, power density, regulation and cross regulation are some of the important requirements in these converters. They can be categorized in to Isolated and Non-Isolated converters. In the non-isolated category, many configurations of single-inductor and multiple-output converters have been discussed in literature [1-13].

A single-inductor, multi-output converter with both buck and boost outputs has been discussed in [5]. Many applications require negative outputs as well but there are not many cases where a negative output has also been obtained in the same converter. [7] proposes a single-inductor triple output converter in all combinations i.e. buck, boost as well as an inverted output [Fig.1]. The inverted output is obtained by feeding power from the load to the source and reversing the direction of the inductor current. The boost output being larger than the supply voltage, after the current feeding the boost output becomes zero, the current direction reverses. This reversed current charges the inductor in the opposite direction and this reverse charged inductor feeds the inverted output. The difficulty in this arrangement is that power flows from the source to the boost output for some time and then back from the boost output to the source. This unnecessary bidirectional transfer of power results in additional losses and an increase in cycle time. Moreover since the current changes direction every cycle, the current ripple is also high.

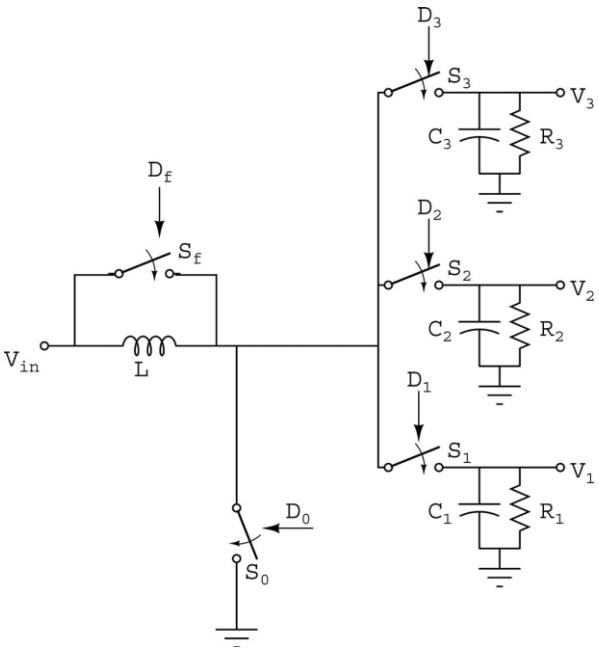

Fig 1.Converter with buck, boost and inverted outputs.

This paper proposes a new improved topology for a single-inductor, triple-output converter with buck, boost and inverted outputs. The converter has only three switches and avoids the problem of reverse power transfer, mentioned above. The inductor current does not have to reverse and operation in continuous conduction mode is possible. The proposed topology is shown in Fig.2 and is explained in the next section. This paper also proposes a simplified predictive-like control of the converter performed by direct analytical estimation of the duty cycle based on the inductor current in the present cycle. This regulates the outputs against supply and load disturbances. The control strategy is discussed in detail in Section 3.

This paper is organized as follows: Section 2 discusses the principle of operation of the proposed converter with its different modes and its steady state analysis. A control strategy based on real-time duty-cycle estimation for the different modes of the converter is discussed in Section 3. The simulation schematic and results are presented in Section 4. Some experimental results are presented in Section 5 and the conclusions are summarized in Section 6.

2.PRINCIPLE OF OPERATION

The proposed converter with buck, boost and inverted outputs is shown in Fig.2. V1 is the boost output, V2 is the inverted output and V3 is the buck output. R1,R2 and R3 are the corresponding load resistances which are paralleled with filter capacitors to reduce the output voltage ripple. For the purpose of analysis, the output capacitor voltages are considered to be constant for a cycle. S0, S1 and S2 are the three switches which could be MOSFETs or IGBTs. The switches could have body diodes as well and D1, D2 and D3 are the three reverse-blocking diodes which prevent conduction in the opposite direction.

Various sequences of operation are possible within a cycle. The sequence chosen here is first buck, then boost and then inverted output. This reduces switching losses since S2 is switched off at zero current. The converter can work well both in continuous and discontinuous conduction modes. The current waveform of the inductor in continuous conduction mode is shown in Figure 3.

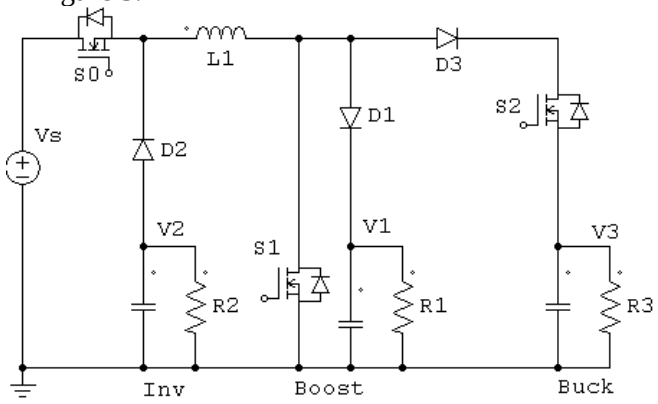

Fig. 2. Proposed buck,boost, inverted output converter

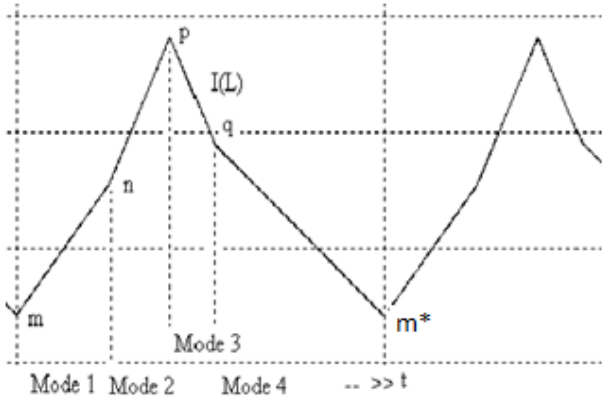

Fig. 3. Inductor current waveform

At the beginning of the cycle the magnitude of the inductor current is denoted as '***m'***. When S2 is switched ON, power is fed to the buck output and the inductor is simultaneously charged. Current rises linearly till '***n'***. At this instant, the energy requirement of the buck output in this cycle has been satisfied. S1 is now switched ON to charge the inductor with the additional energy required for the boost and inverted outputs. The current in the buck switch will become zero after which it is can be switched off at zero current. The current rises linearly to '***p***'. At this instant, the inductor together with the source has sufficient energy to supply the boost and inverted outputs. S1 is now switched off and power is fed to the boost output. The boost output does not have a separate switch and current from the inductor flows through the diode D1 to the boost output.

When the current has fallen to '***q***' the boost output has been serviced. S0 is now switched off and the inductor current discharges in to the negative output through D2 and reaches '***m*'*** at the end of the switching period. In steady state, '***m*'*** would be same as '***m'*** and the cycle repeats. For operation in discontinuous mode, '***m*'*** would be zero, and after a dead time the cycle would repeat. The modes of operation with the corresponding diagrams and steady state equations are discussed below:

Mode 1(Fig. 4a)

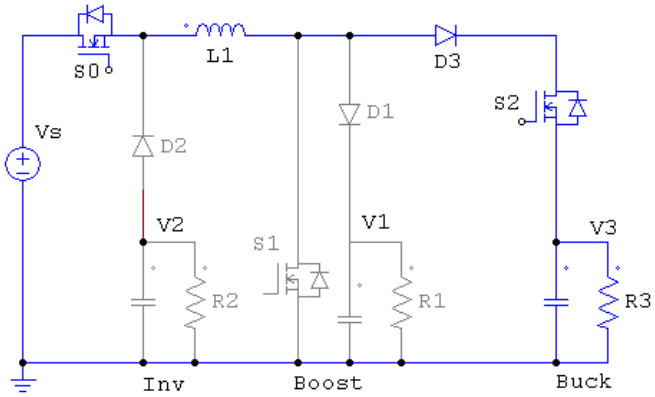

Fig. 4a. Equivalent circuits for Mode 1

Initially, at the beginning of the cycle, the switches S0 and S2 are turned ON and the inductor L1 is charged. Simultaneously the buck output is also fed power. The current in the inductor rises linearly from the initial value '***m'*** to '***n'*** after duration d1*Ts where Ts is the switching time period and d1 is the duty cycle of mode 1.The inductor current equation for this mode is

$$(n-m)=(V_s-V_3)d_1T_s/L \qquad (1)$$

Or $$n=m+(V_s-V_3)d_1T_s/L \qquad (2)$$

The average inductor current during Mode 1 times d1 is the average current supplied to the buck output during a cycle.

$$(n+m)d_1/2=V_3/R_3=a \qquad (3)$$

$$(n+m)=2a/d_1 \qquad (4)$$

From (1) and (4),

$$n^2-m^2=2aT_s(V_s-V_3)/L \qquad (5)$$

$$n=\sqrt{m^2+2aT_s(V_s-V_3)/L} \qquad (6)$$

Mode 2 (Fig. 4b)

In mode 2, the switch S1 is turned on and switch S2 is turned OFF. S0 remains ON. The turning ON of S1 can even precede turn off of S2 such the ZCS of S2 is obtained. The inductor L1 rises linearly and is charged sufficiently for duration d2*Ts to take care of the requirements of the boost and the inverted outputs in the subsequent modes. After d2*Ts, the inductor current magnitude reaches a value '***p***'. The diode D3 prevents a reverse flow of current from the buck output. The inductor current for this mode is

$$(p-n)=V_s d_2 T_s / L \qquad (7)$$

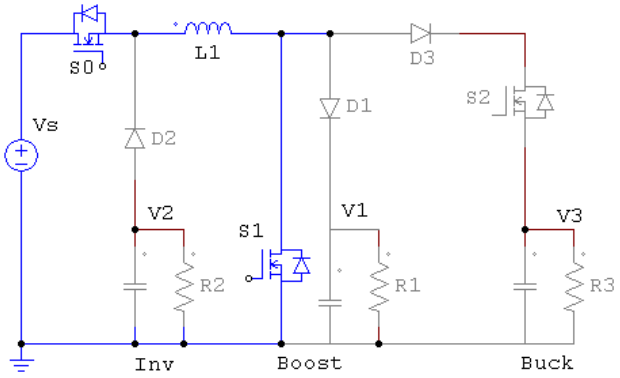

Fig. 4b. Equivalent circuits for Mode 2

Mode 3 (Fig. 4c)

In this mode, the switch S1 is turned OFF. The inductor current discharges in to the boost output through diode D1 for duration d3Ts and the current falls linearly from '***p***' to '***q***'.

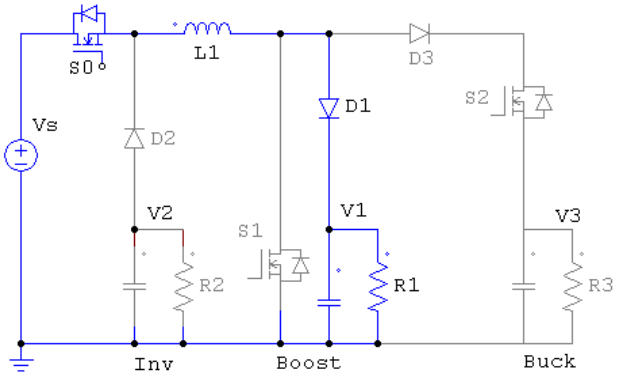

Fig. 4c. Equivalent circuits for Mode 3

The inductor current equation for this mode is

$$(q-p)=(V_s-V_1)d_3 T_s / L \qquad (8)$$

The average inductor current during Mode 3 times d3 is the average current supplied to the boost output in a cycle.

$$(p+q)d_3/2=V_1/R_1='b' \quad \text{and hence}$$

$$(p+q)=2b/d_3 \qquad (9)$$

From (8) and (9),

$$(q^2-p^2)=2b(V_s-V_1)T_s/L \qquad (10)$$

$$q=\sqrt{p^2+2b(V_s-V_1)T_s/L} \qquad (11)$$

Mode 4 (Fig. 4d)

At the end of Mode 3 when current magnitude becomes 'q' and the boost output is satisfied, S1 is turned ON and S0 is turned off. The inductor current flows through S1 in to the inverted output. After duration d4*Ts, the current becomes '***m****'. In steady state, '***m****' would be same as '***m***'. The inductor current equation for this mode is

$$(m*-q)=-V_2 d_4 T_s / L \qquad (12)$$

$$d_4=1-d_1-d_2-d_3 \qquad (13)$$

The average inductor current during Mode 4 times d4 is the average current supplied to the inverted output in a cycle.

$$(m*+q)d_4/2=V_2/R_2='c' \qquad (14)$$

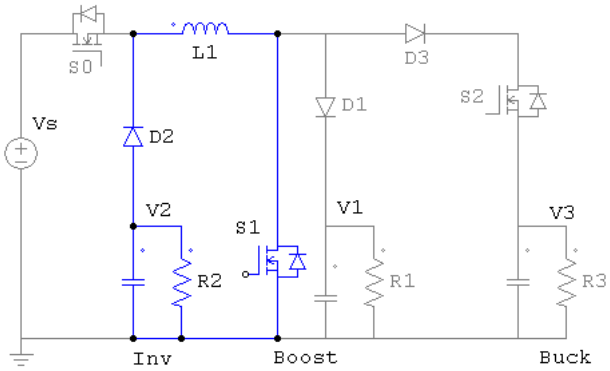

Fig. 4d. Equivalent circuits for Mode 4

There are 4 mode equations and three output equations making it in to 7 equations. At steady state, '***m****' is same as '***m'***. From (13), d4 is found and hence both the variable d4 and the equation (13) are not considered. There are 8 unknown variables, d1, d2, d3, m, n, p, q and (Ts/L). Current ripple would be less for large inductance and small time period and hence for small values of (Ts/L). Using any iterative software, typical values can be found by applying suitable constraints.

3.CONTROL STRATEGY

The outputs of the proposed converter are regulated against line and load variations by a predictive-like valley current control. In predictive control, the variables of the present cycle are used to predict the variables for the next cycle[14]. In the proposed strategy, the prediction is done by a direct analytical estimation of the duty cycle for the next cycle based on the inductor current and duty cycles of the present cycle, and the required power demand. The current in the beginning of the present cycle is obtained either by measurement with a sensor or by estimation. The average current demand of the outputs is obtained using PI regulators for each of the outputs. From the

present value of the inductor current and the present duty cycle values, the inductor current at the beginning of the next cycle is analytically estimated. With this information, the duty cycles of the next cycle are predicted so as to satisfy the current demand of the outputs. This would in turn bring the output voltages to the required values. The different steps involved in the current control are listed as follows:

(i) The output voltages V1, V2 and V3 are measured. The actual inductor current is also measured at the beginning of the cycle. This corresponds to '***m***'. Each of the outputs (buck, boost and inverted) is compared with its set point and the error is passed through a PI regulator. The output of the PI regulators corresponding to buck, boost and inverted outputs after suitable limiter blocks are termed as 'a', 'b', and 'c' respectively.

(ii) **Finding d1 :**'***n***' can be found from (6) since all other values are known and output voltages are known from (i). Since both '***n***' and '***m***' are known, d1 can be obtained from (1) as

$$d_1 = \{(n-m)L\}/\{(V_s - V_3)T_s\} \quad (15)$$

(iv) **Finding d2 :**The average supply current demand (i_s) can be estimated from power balance considerations as

$$i_s = (aV_3 + bV_1 + cV_2)/V_s \quad (16)$$

The average mode 2 current over a complete cycle is defined as 'K' as

$$K = (p+n)d_2/2 \quad (17)$$

Average inductor current

$$i_L = (a+b+c+K)$$

and since average current to the negative output, 'c', does not flow from the supply directly,

$$K = i_s - (a+b) \quad (18)$$

Since from (7),

$$p = n + (V_s T_s d_2)/L \quad (19)$$

substituting in (17),

$$K = \{n + (V_s T_s d_2)/2L\}d_2 \quad (20)$$

$$\{(V_s T_s d_2^2)/2L\} + (nd_2) - K = 0 \quad (21)$$

from which d2 can be obtained as

$$d_2 = \{-n + \sqrt{n^2 + (2V_s T_s K)/L}\}/(V_s T_s/L) \quad (22)$$

(v) F**inding d3**

Since 'n' and d_2 are already found, '***p***' can be found from (19), $p = n + (V_s T_s d_2)/L$ and from (11),

$$q = \sqrt{p^2 + 2b(V_s - V_1)T_s/L}\,.$$

From (9), d3 can be obtained as

$$d_3 = 2b/(p+q) \quad (23)$$

For continuous conduction, d4 is the balance time left in the cycle,

$$d_4 = 1 - d_1 - d_2 - d_3 \quad (24)$$

4. SIMULATION & RESULTS

The specifications of the chosen converter are given in TABLE 1. The power and control schematic diagram as simulated in PSIM is shown in Fig.5a. The expanded subsystem control block is shown in Fig.5b. The simulation results are shown in Fig.6a to 6g.

TABLE I

SPECIFICATIONS OF CONVERTER

Supply Voltage	12V
Switching frequency	50KHz
Output 1	24V,40 Ω
Output 2	-5V, 10 Ω
Output 3	+5V, 10 Ω

The switch and inductor currents are illustrated in Fig.6a. The duty cycles for the 4 modes d1, d2, d3 and d4 and the output voltages V1, V2 and V3 are shown in Fig.6b. The output voltages are held at the specified values without any steady state ripple.

From the simulation waveforms, it can be seen that the output voltages are tightly regulated against load and supply variations and cross regulation is very minimal. For a change in load resistance R3 from 5 to 10 and then 15 ohms while keeping R1 and R2 same, Fig.6c shows that the three outputs continue to be closely regulated at the required values.

Y axis is shown in an expanded scale and the variation in the three output voltages for a change in the load resistance R3 from 5 to 15 ohms is less than 0.01V (0.2%). Similarly the regulation of the three outputs for a variation in R2 from 5 to 15 ohms is shown in Fig.6d and the regulation of the three outputs for a variation in R1 from 30 to 50 ohms is shown in Fig.6e. In all cases, the regulation is better than 0.5%.

When the supply voltage of 12V changes by 20% from 9.6V to 14.4V, all the the outputs are still regulated closely as seen in Fig.6f. The ripple on the output voltages is less than 5% and the regulation is better than 0.2%.

The transient regulation for a sharp change in one of the loads and in the supply is illustrated in Fig.6g to Fig.6j at different time instants. The sampled current at the beginning of the cycle and the output voltages for a step change in buck output load resistance from 15 to 5 ohms at the 25^{th}ms is illustrated in Fig.6g. The output voltages for a step change in the boost output load resistance from 50 to 30 ohms at the 35^{th}ms is illustrated in Fig.6h. The output voltages for a step change in the inverted output load resistance from 15 to 5 ohms at the 45^{th}ms, is illustrated in Fig.6i. The output voltage for a step change in the supply voltage from 12 to 15V at the 50^{th} ms is shown in Fig.6j. It is seen that the output voltages are closely regulated in all these cases for supply and load variations. The mutual coupling interference between the outputs during this sharp load changes is also seen to be minimal.

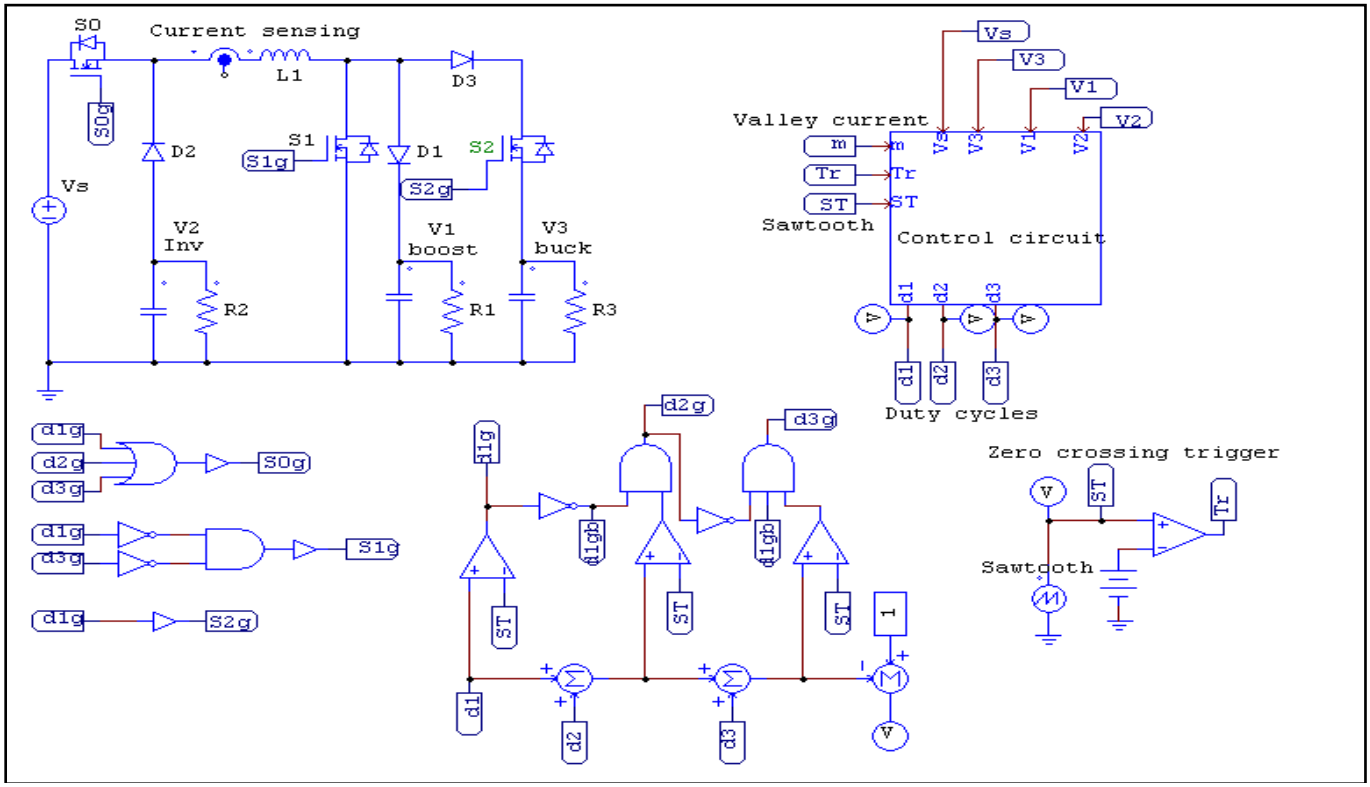

Fig.5a Power and Control schematic

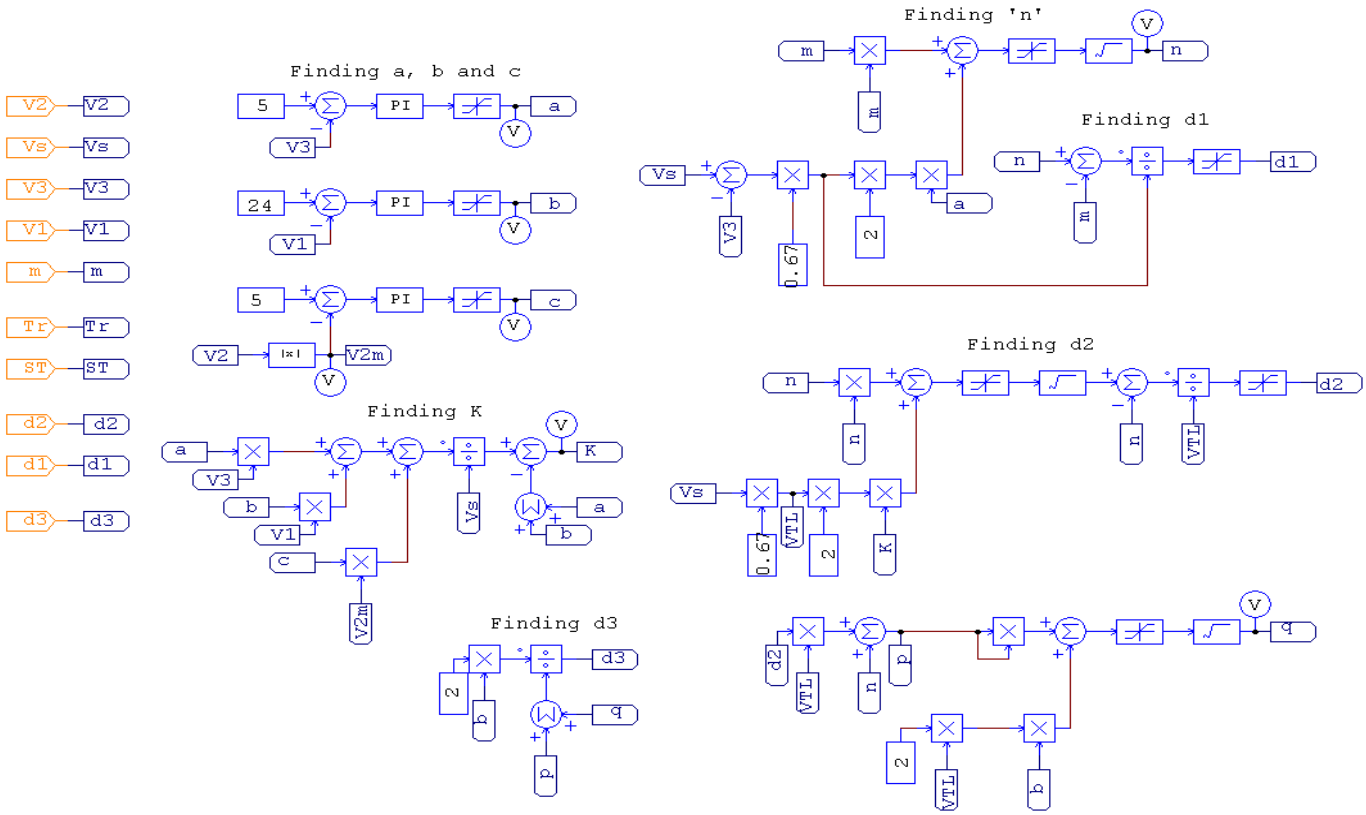

Fig.5b Expanded control circuit block

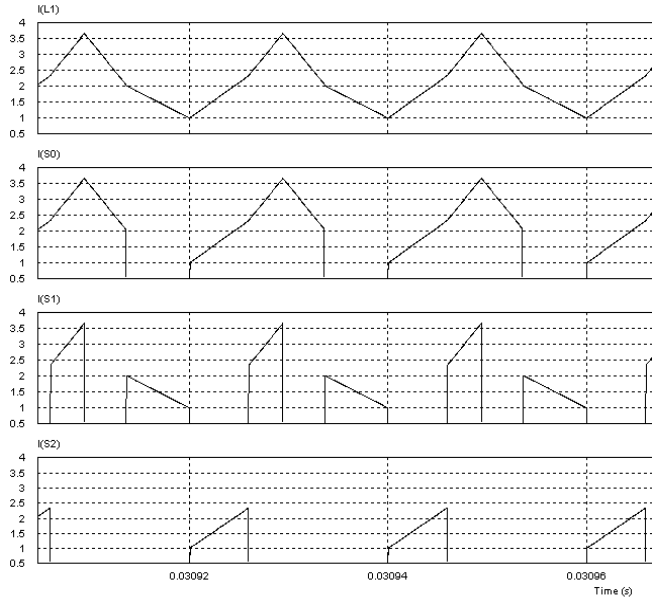

Fig.6a Switch and Inductor currents

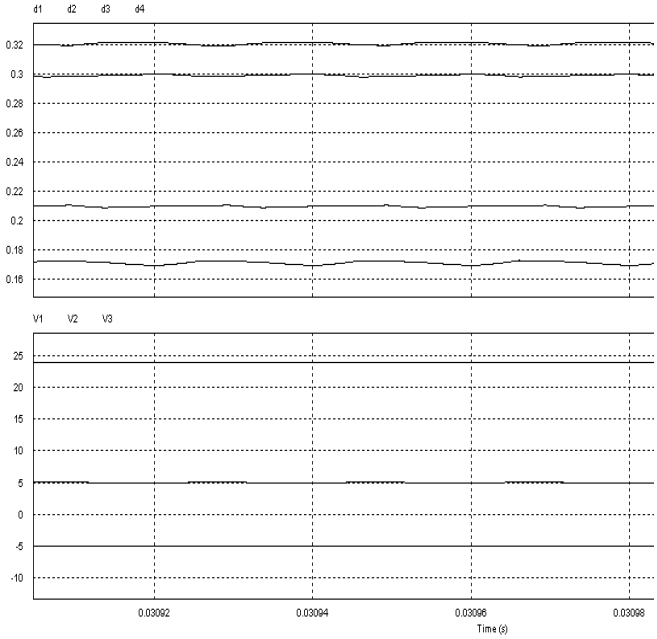

Fig.6b Duty cycles during the 4 modes and outputs

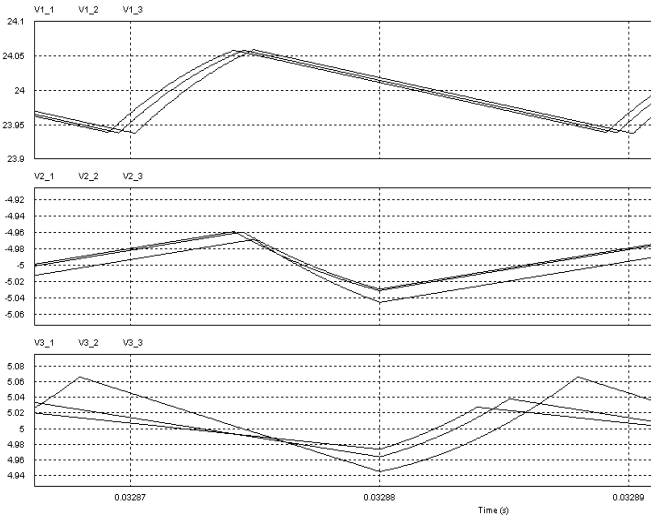

Fig.6c Output Voltages for R3=5, 10 and 15 ohms

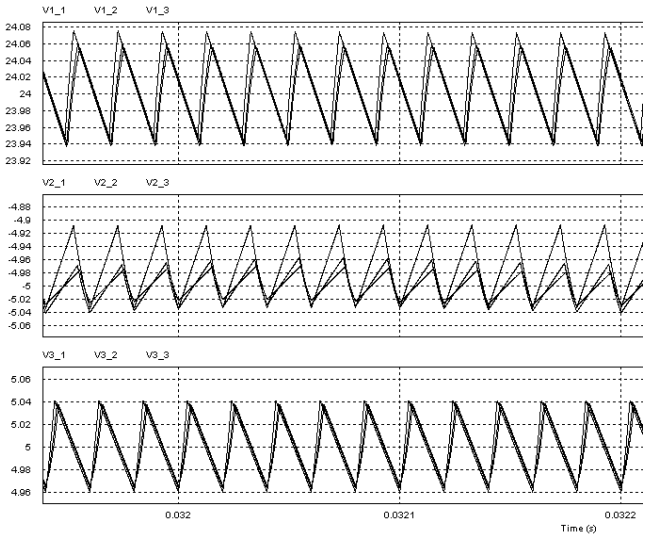

Fig.6d Output Voltages for R2=5, 10 and 15 ohms

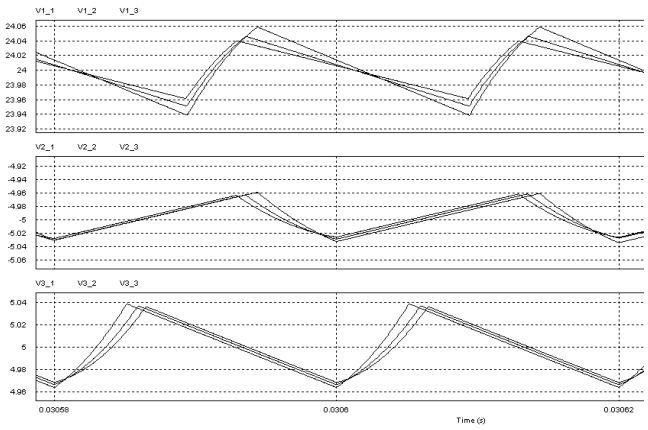

Fig.6e Output Voltages for R1=30, 40 and 50 ohms

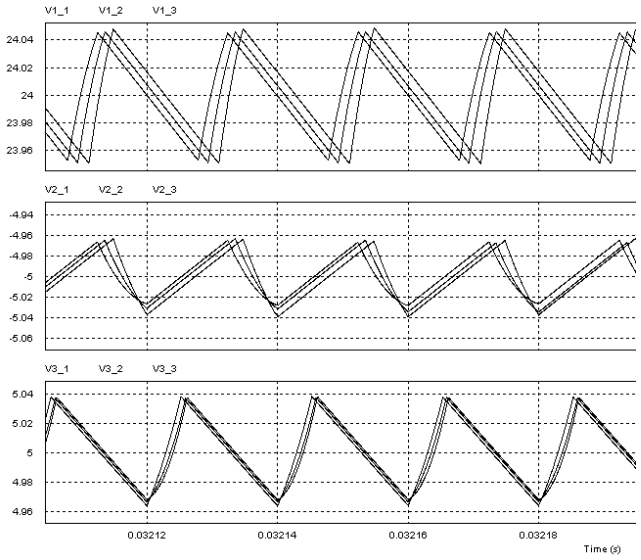

Fig.6f Output Voltages for Vs=9.6V,12V and 14.4V

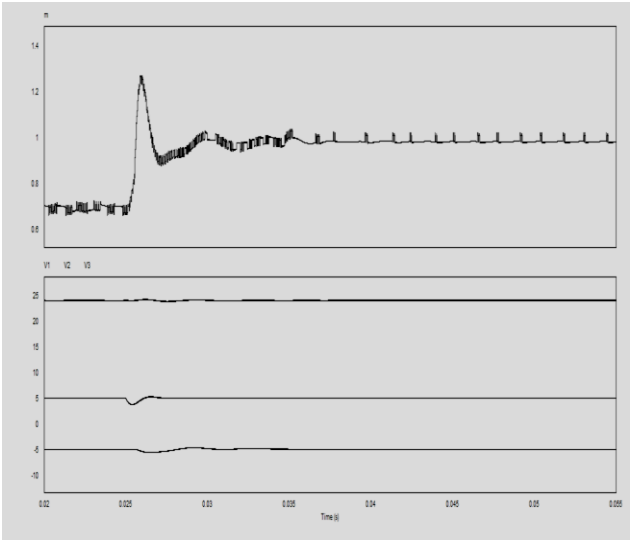

Fig.6g Inductor current, output voltages for step change in buck load resistance from 15 to 5 ohms at 25thms

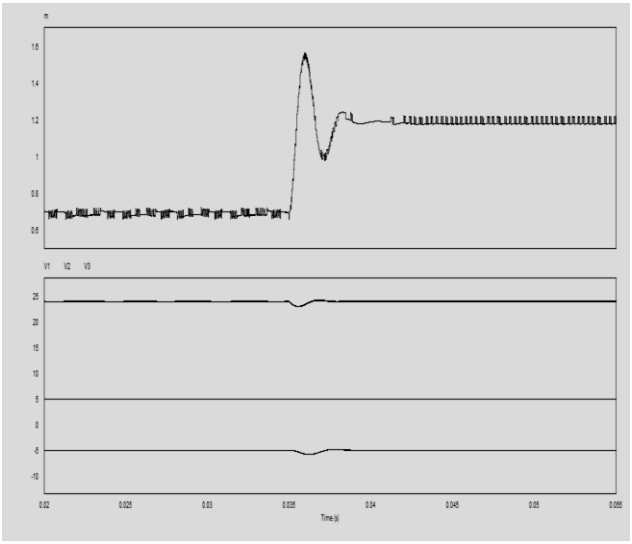

Fig.6h Inductor current, output voltages for step change in boost load resistance from 50 to 30 ohms at 35thms

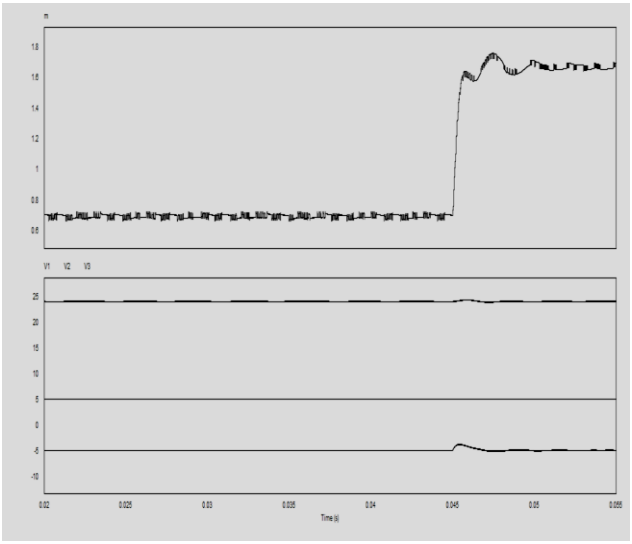

Fig.6i Inductor current, output voltages for change in Inverted output resistance from 15 to 5 ohms at 45thms

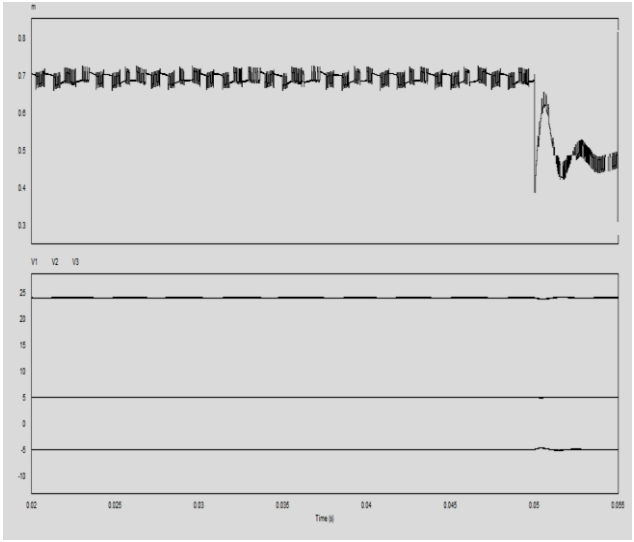

Fig.6j Inductor current, output voltages for change in supply voltage from 12 to 15 ohms at 50th ms

5. EXPERIMENTAL RESULTS

For an experimental validation of the concept, the hardware implementation of the triple output converter in open loop was implemented using a Spartan FPGA XC3S250 system. The clock frequency of the FPGA is 20MHz which corresponds to a time period of 50ns. IRF 840 was used for the MOSFET switches. The duty cycles obtained from simulation was used to drive the MOSFET switches during different intervals. Appropriate numbers of clocks are calculated for each time interval. The waveforms of the pulses to the switches is shown in Fig.7a. The inductor current, buck switch currents and current through switch S1 are shown in Fig.7b to Fig.7d. The buck, boost and inverted output voltages are illustrated in Fig.7e to Fig.7g. The waveforms are in line with the expected pattern and match with the simulation waveforms. An image of the hardware setup used for the testing is shown in Fig.7h.

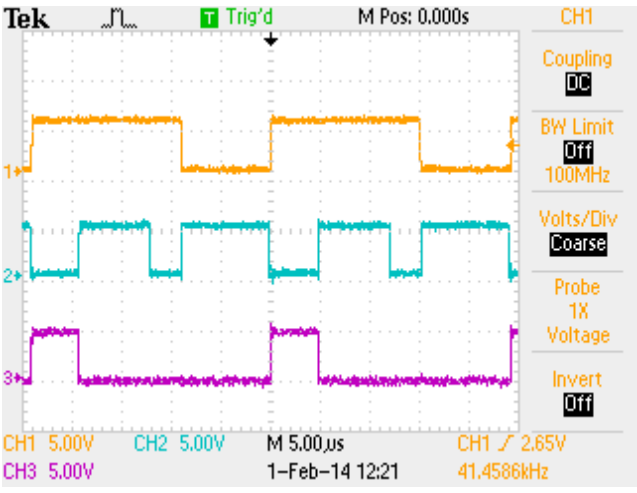

Fig.7a Pulses to the three switches

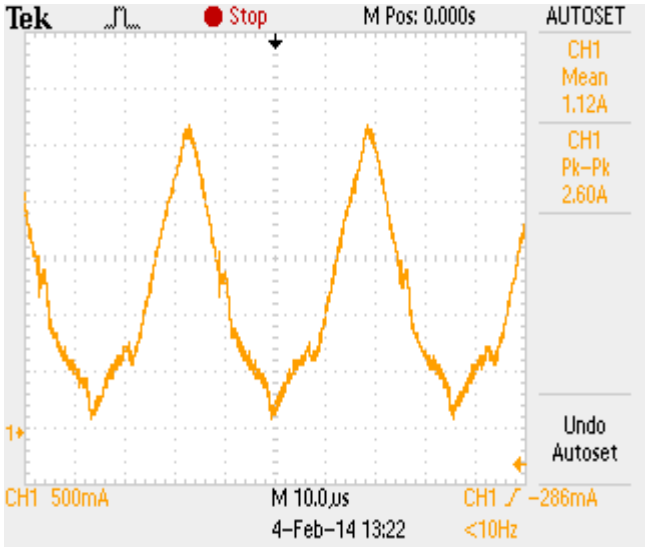

Fig.7b Inductor current

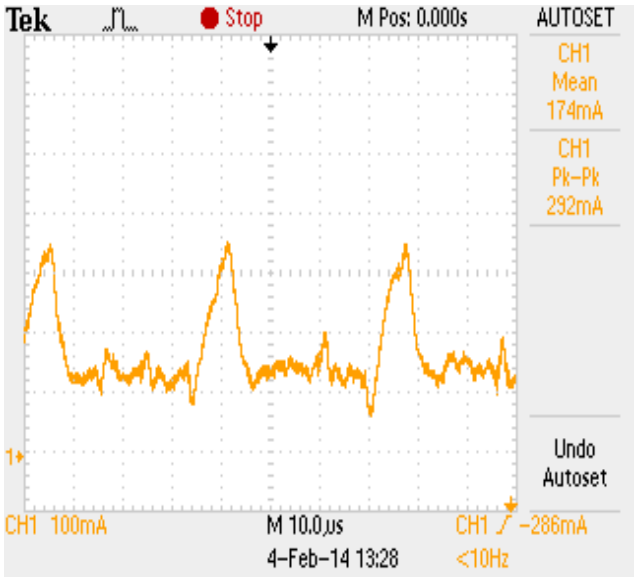

Fig.7c Buck switch current

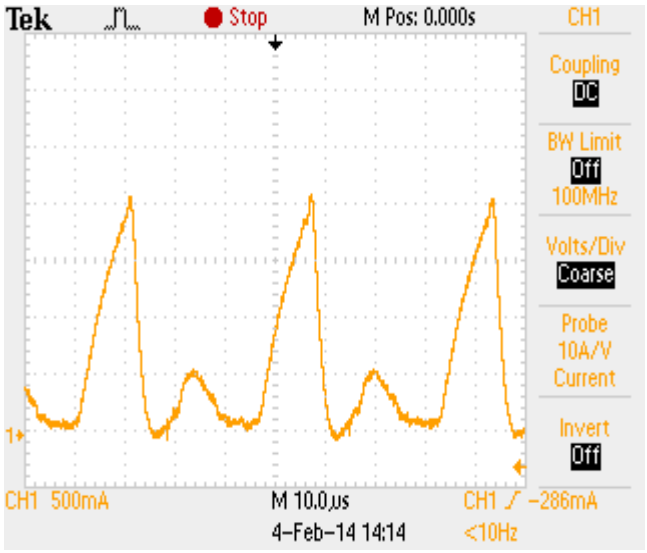

Fig.7d Current of switch S1

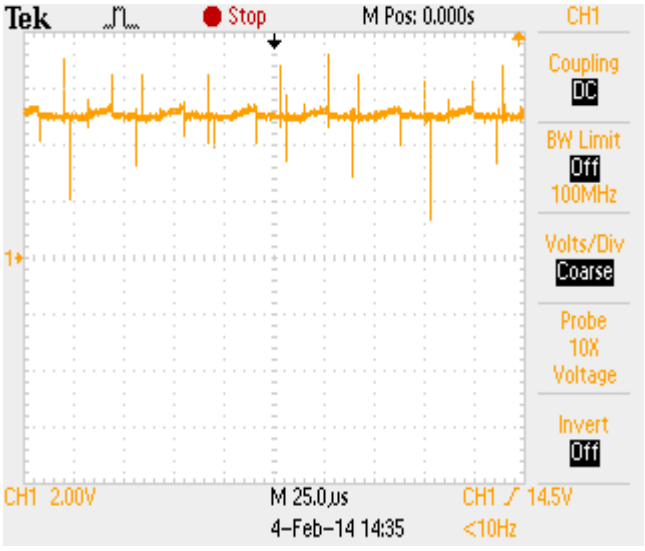

Fig.7e Buck output voltage

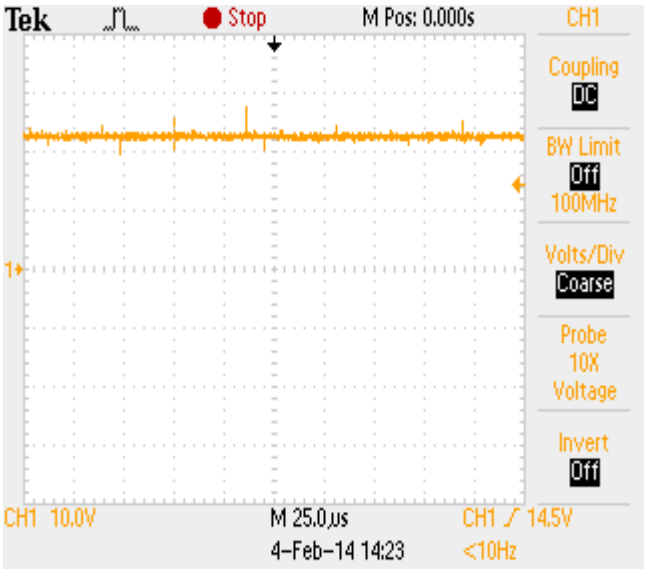

Fig.7f Boost output voltage

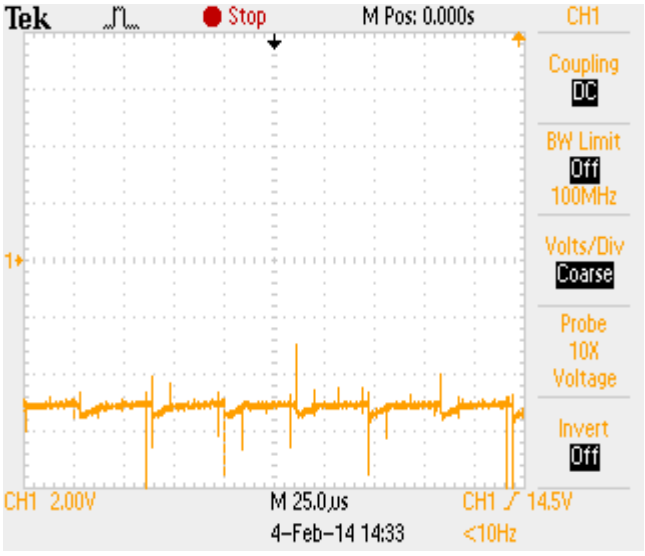

Fig.7g Inverted output voltage

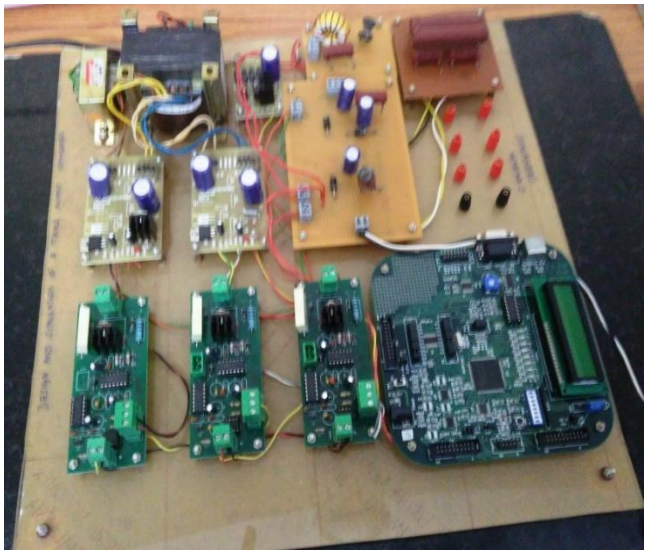

Fig.7h Image of the hardware setup

6. CONCLUSION

This paper discussed a triple output converter with only three switches and with a unidirectional power flow from the supply towards the output. No reversal of inductor current was required for obtaining the negative output. A simplified predictive control strategy with analytical estimation of duty cycles has been discussed for real time calculation of duty cycles. Cross regulation between the outputs is minimal and the output voltages are closely regulated for widely varying supply voltages and loads.

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